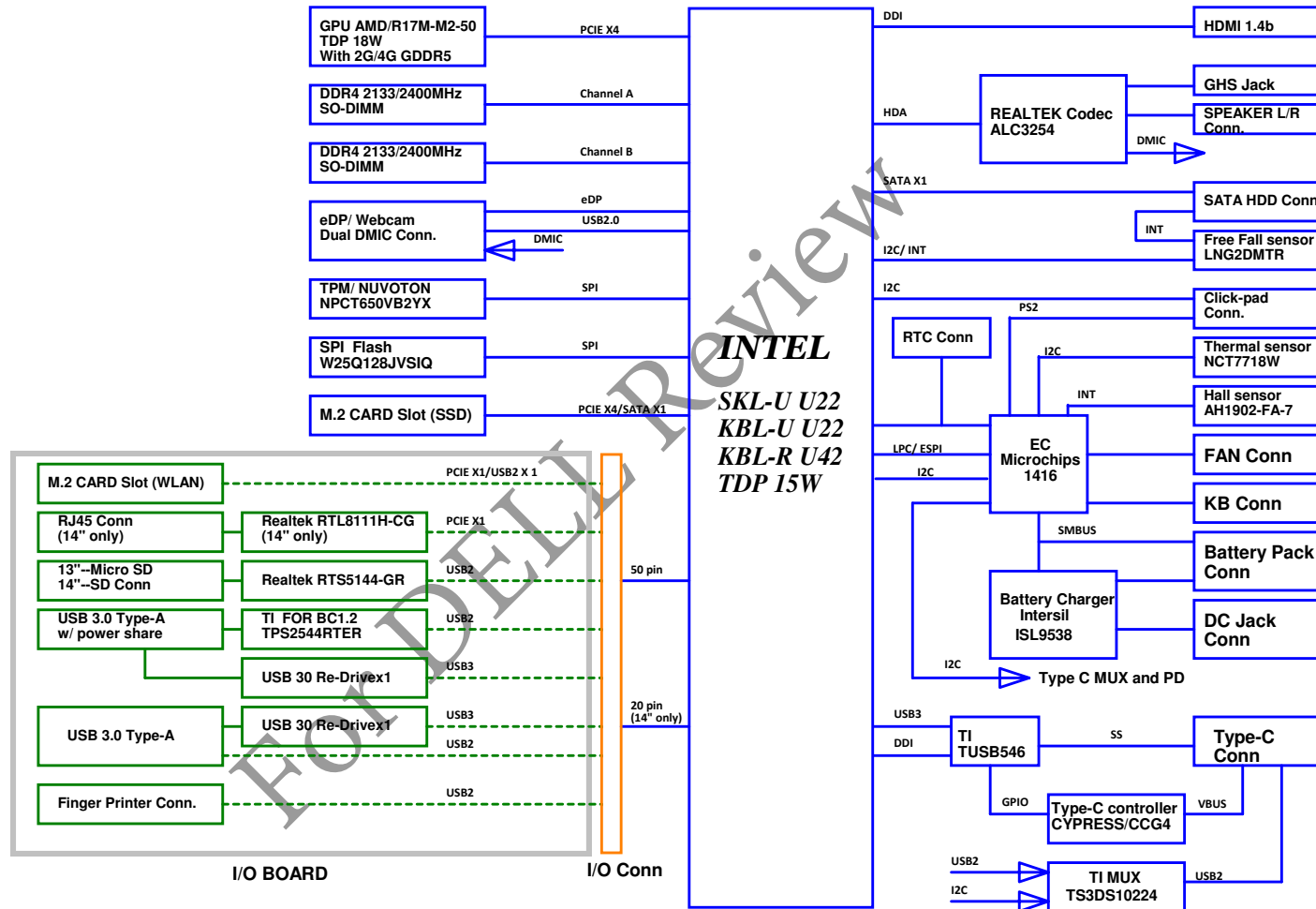
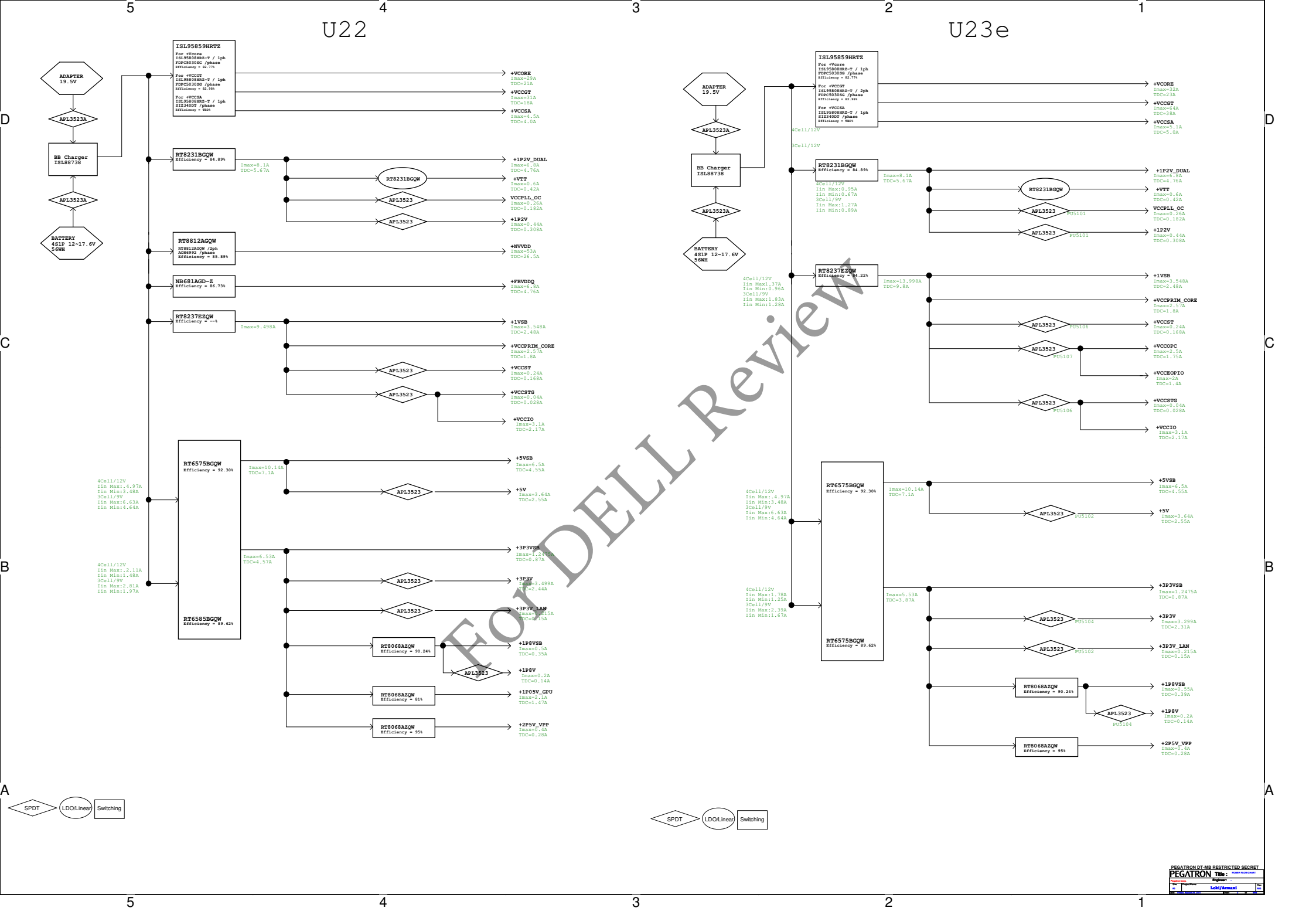
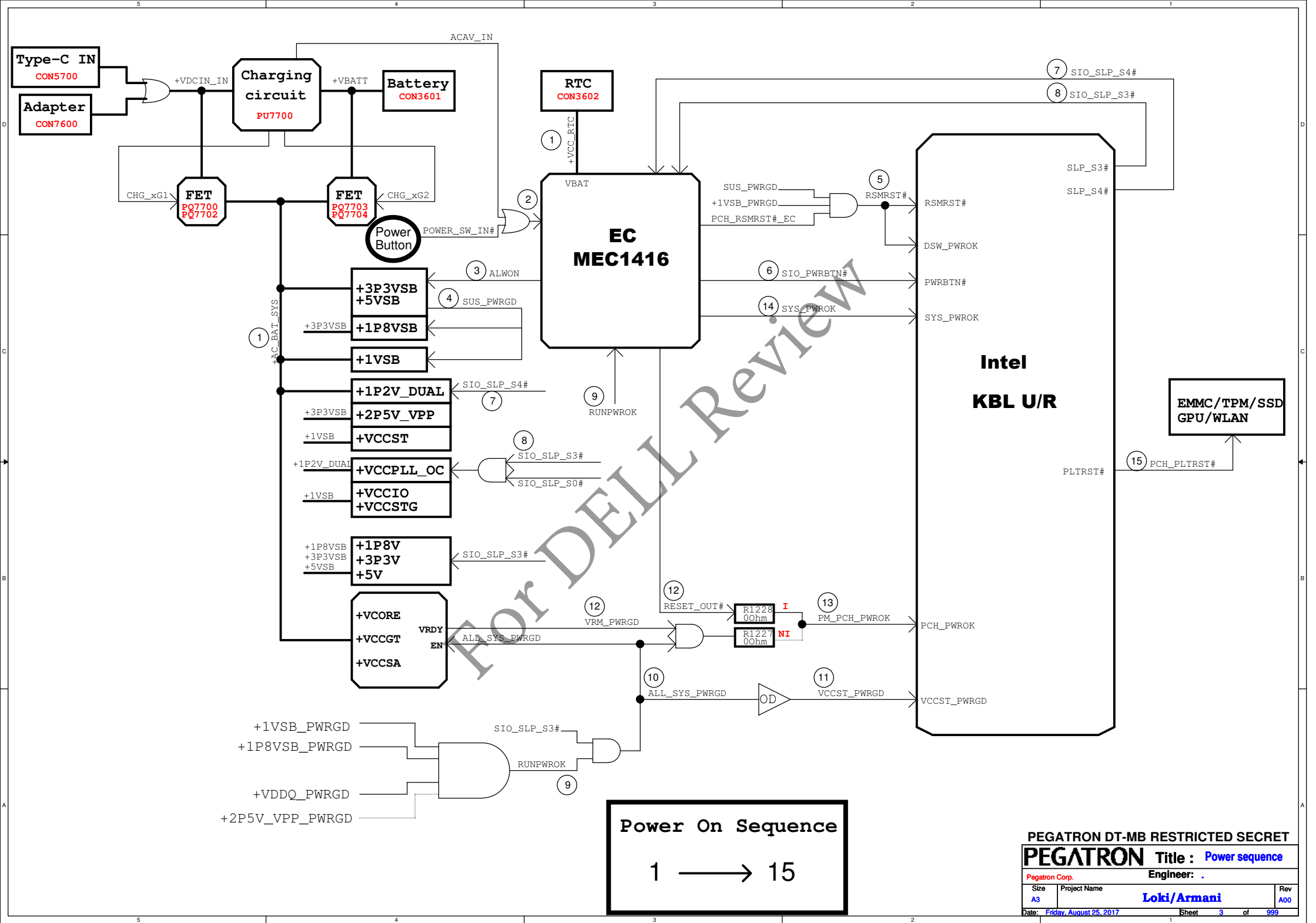


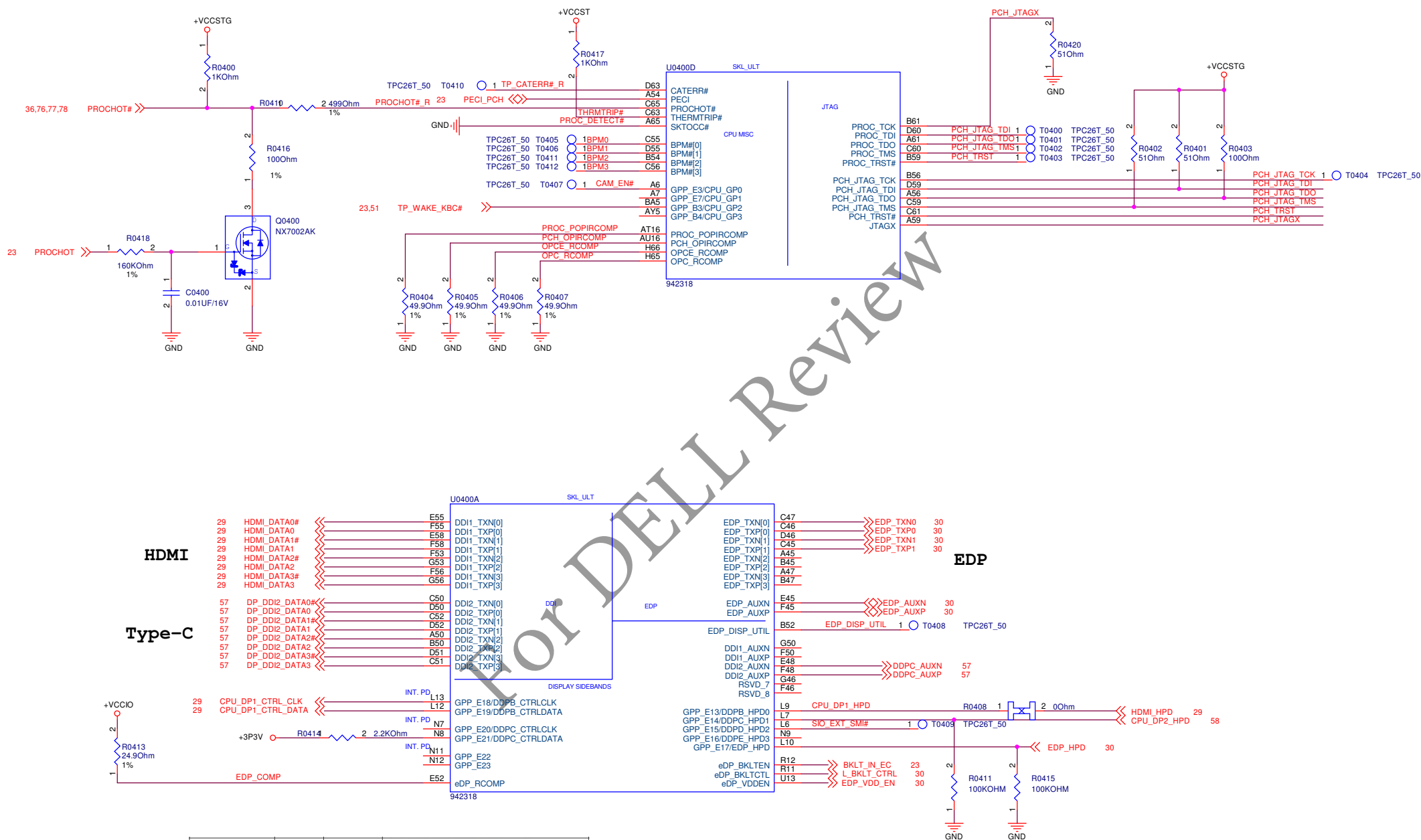
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02. POWER_FLOW_CHART
03. Power_sequence
04. CPU(1)_MISC,JTAG,DDI. EDP
05. CPU(2)_DDR4
06. CPU(3)_SKL_POWER1
07. CPU(4)_SKL_POWER2
08. CPU(5)_GND
09. CPU(6)_CFG_RESERVED
10. PCH(1)_SD,HDA,RTC,CLK
11. PCH(2)_CLK,SMB,LPC,SPI
12. PCH(3)_SYS_PWR_CONTR
13. PCH(4)_CCI,HWDI
14. PCH(5)_PCIE,USB
15. PCH(6)_CPU,GPIO,MISC
16. PCH(7)_POWER
18. PWRGD_DETECT
19. SPI_ROM&SM_BUS
20. DDR4_SO-DIMM0
21. DDR4_SO-DIMM1
22. DDR4_TERMINATION_A&B
23. EC#1
24. EC#2
25. EMMC
26. HDMI_CON
29. HDMI14b
30. eDP
31. M.2_2280_SSD/HDD
36. Battery&FANConn
37. Sensor
38. AUDIO_ALC3254
39. TPM
50. LED
51. Keyboard&iO_connector
52. Screw_Hole&Nut
53. DEBUG
57. Type-C_MUX
58. Type-C_PD
59. VBUS_Provider
60. AMD_DGPU_PCIEX8
61. AMD_DGPU_IFPA/B_LVDS
62. dGPU_STRAPS
63. AMD_DGPU_FBA_CHA
64. AMD_DGPU_FBA_CHB
65. dGPU_FBVDDQ
66. dGPU_MEMORY_DECOUPLING
67. AMD_VDD
68. dGPU_MEMORY_UPPER
69. dGPU_BIOS
70. AMD_DGPU_THERMAL/GPIO/JTAG
71. dGPU_DP&DVI&HDMI
72. GPU_POWER_DISCHARGE_CIRCUIT
76. DC_IN
77. BB_Charger
78. CPU_CONTROLLER
79. +VCORE
80. +VCCGT/VCCSA
81. VR_CAPACITORS
82. +VCCIO
83. +VCCPRIM_CORE
84. +VCCEDRAM
85. +VCCOEPIO
86. +1P2V_DUAL/+VTT_DDR
87. +1VSB
88. +1P8V/+2P5V_VPP
89. +3VA/5VSB
90. Load_Switch_1
91. Load_Switch_2
92. Load_Switch_3
93. LDO1
94. +VDDC_CONTORLLER
95. 1.8V/ 0.95V_VGA
96. +VDDC_OUTPUT
97. XXXXXX
98. FBVDDQ

Block Diagram









DDPC_CTRLDATA/ GPP_E21	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected, (Default) 1 = Port C is detected. Notes: 1. The internal Pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
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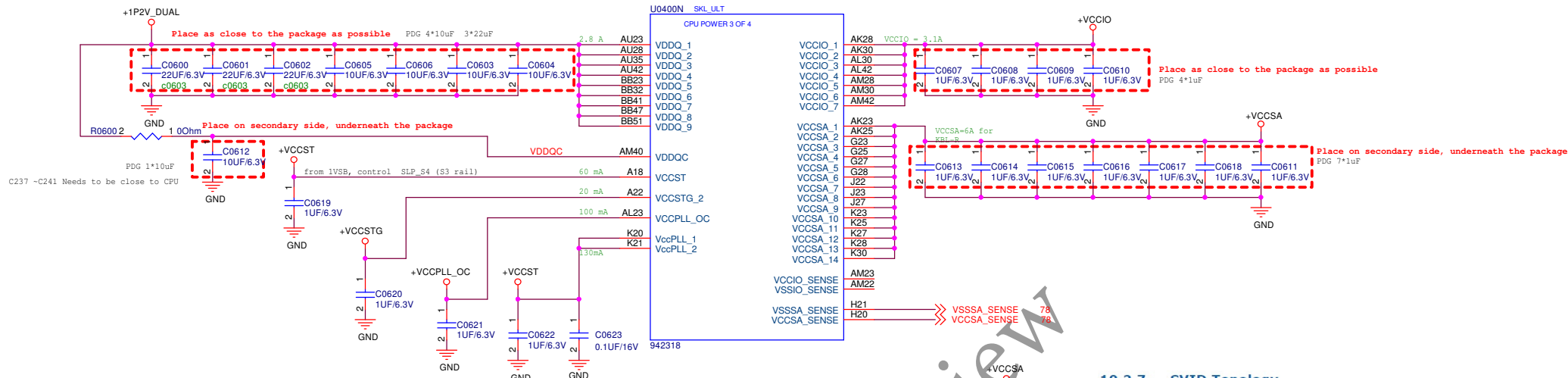
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU(1)_MISC,JTAG,DDI

Pegatron Corp. Engineer: .

Size A3 Project Name **Loki/Armani** Rev A00

Date: Friday, August 25, 2017 Sheet 4 of 999



10.2.7 SVID Topology

Figure 10-5. Routing Illustration for SVID Topology

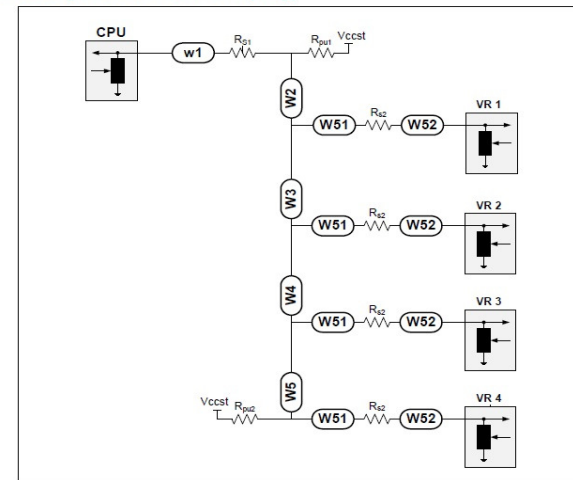


Table 10-8. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R ₀₁ [Ω]	R ₀₂ [Ω]	R ₀₃ [Ω]	R ₀₄ [Ω]	VCC _{ST} [V]
VIDSOUT							100	100	0	10	
VIDSCK	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	0	50	1.0
VIDALERT #							56	Empty	220	0	

Note: For additional information regarding SVID and power management refer to Chapter 47, "Power Architecture Guide" in this document.

Table 10-9. SVID Minimum Spacing Guidelines

Coupling length [inches]	Stripline [mils]	Microstrip [mils]
<0.5	5	5
<2.5	10	10
>2.5	12	15

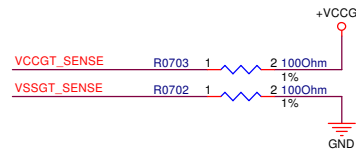
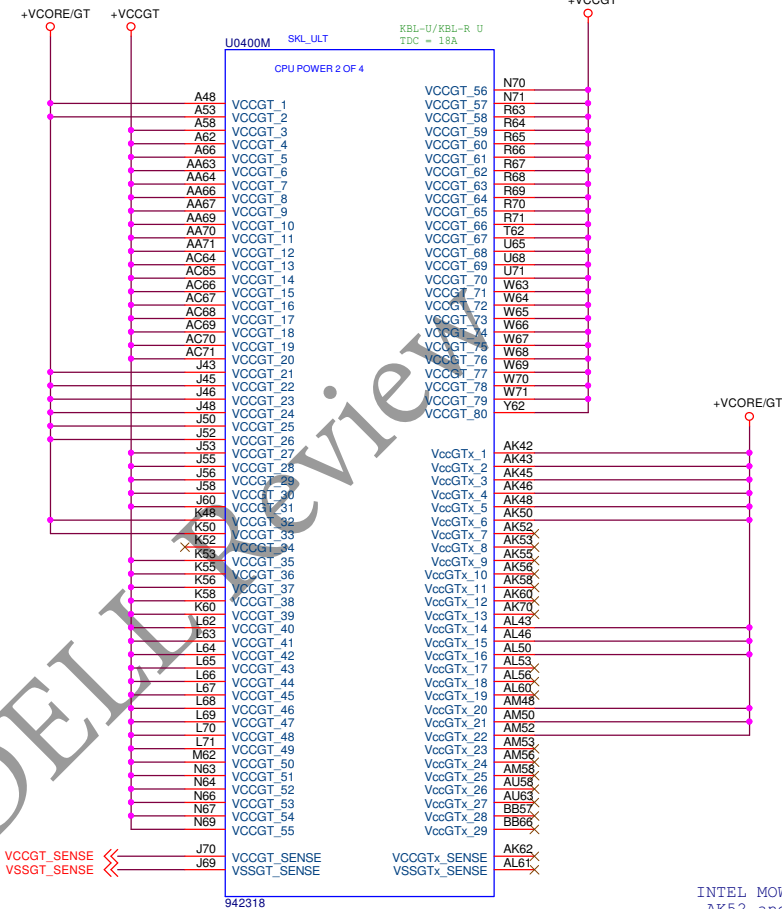
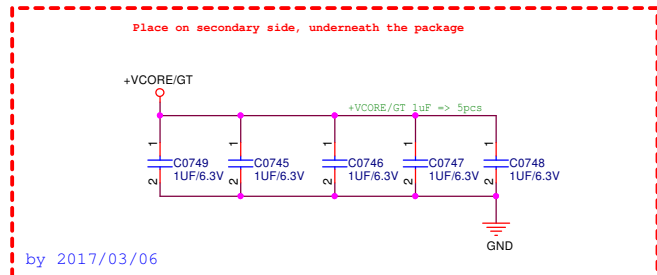
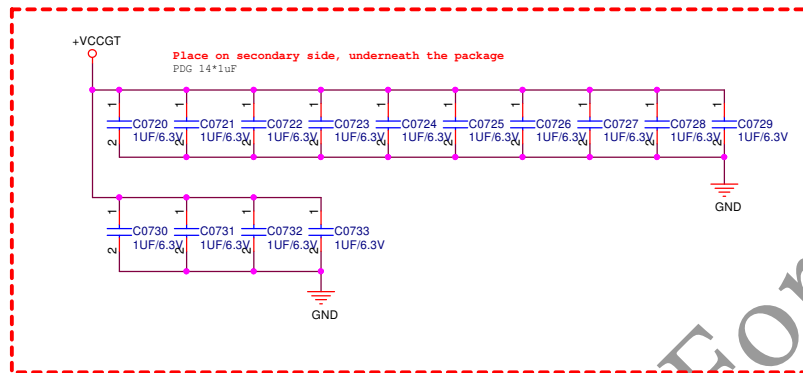
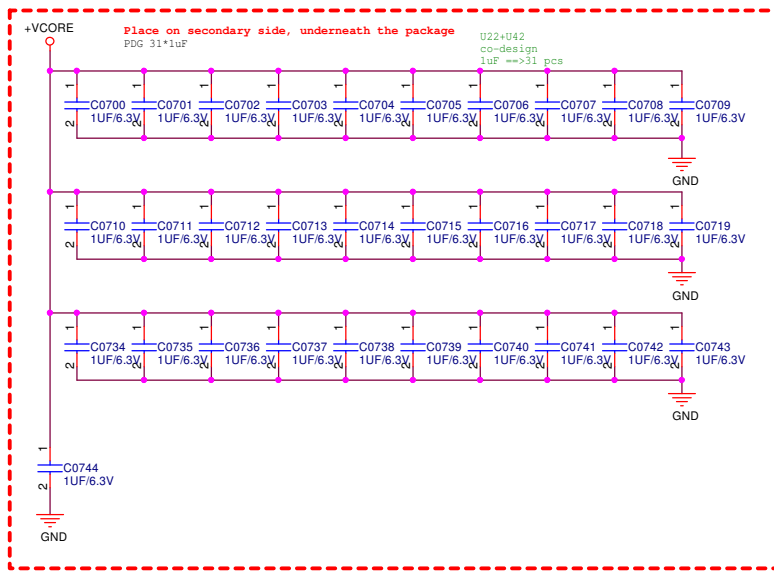
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU(3)_SKL POWER1

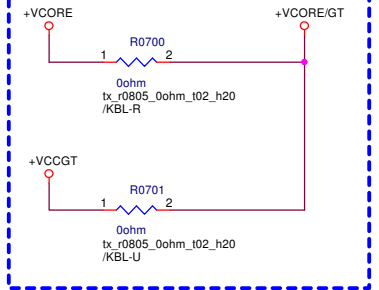
Pegatron Corp. Engineer: .

Size A3 Project Name Loki/Armani Rev A00

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KBL-U U22 & KBL-R U42 BOM change



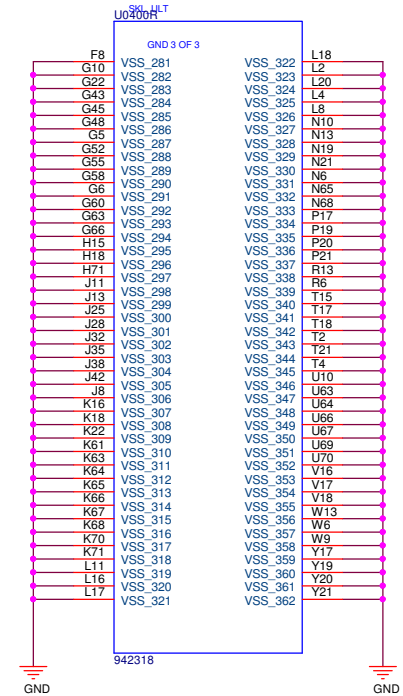
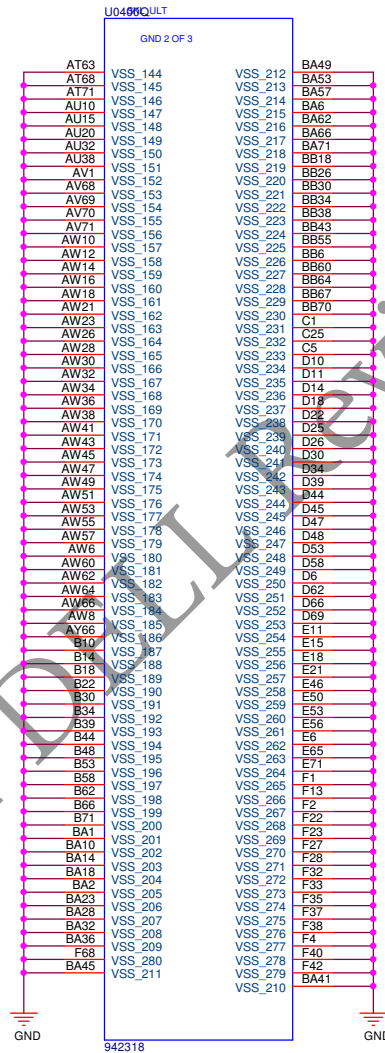
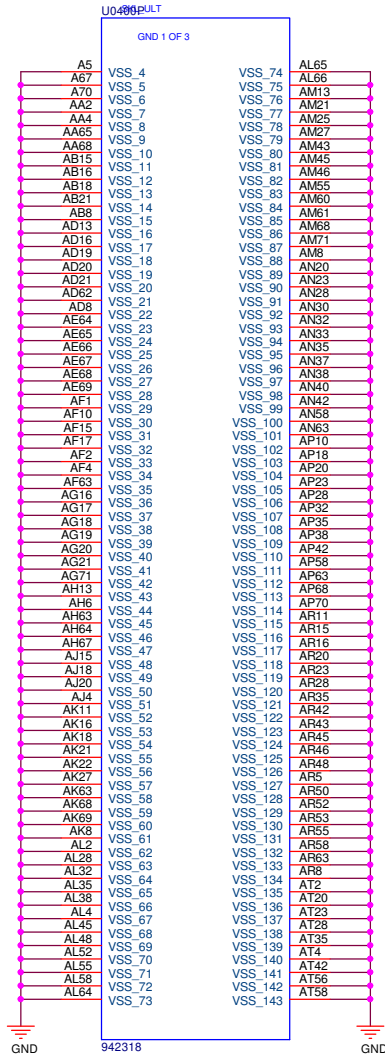
INTEL MOW WW09, March 2017 update
AK52 and K52 Keep NC

1.1.2 Kaby Lake U AK52 and K52 Kaby Lake Silicon Ball Connectivity Recap from PDG (568813_KBL_R_U42_PDG_Addendum_Rev0p9, Page 12)

Description:

Please ensure to follow the below Connectivity guidelines on AK52 and K52 Kaby Lake Silicon Balls for Compatible Design (KBL-R U42/KBL U22/KBL U23e).

KBL-R U42 Only Design	Do not Connect AK52 and K52 Balls, Keep as NC
KBL-R U42 Compatible Design for (KBL-R U42/KBL U22/KBL U23e) Support	Do not Connect AK52 and K52 Balls, Keep as NC



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU(5)_GND

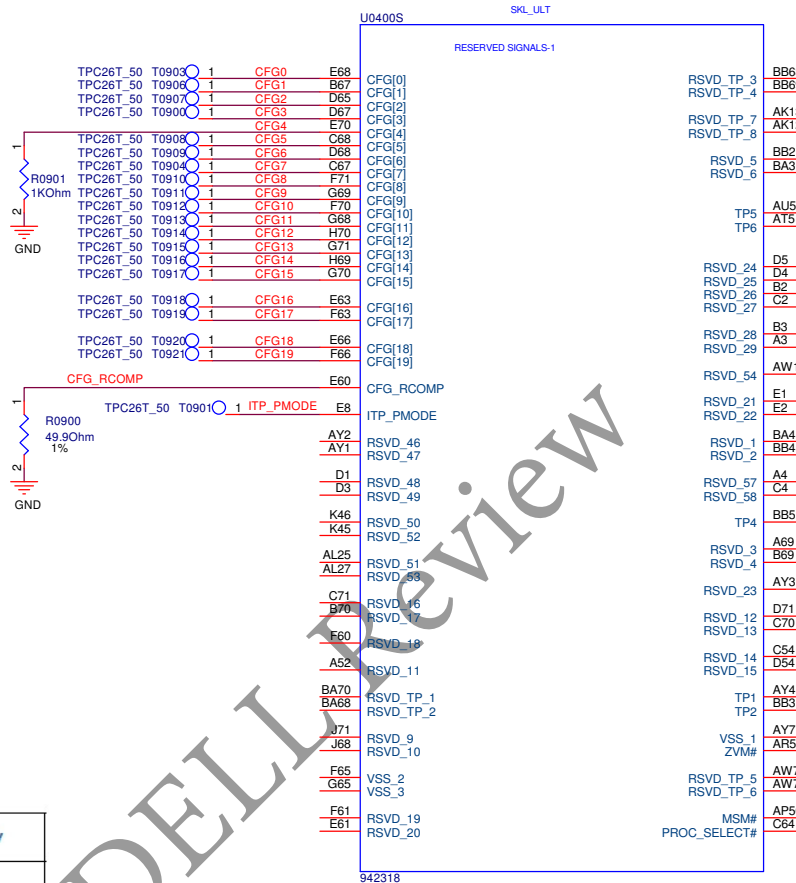
Pegatron Corp. Engineer: .

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CFG4		
0	Default	Enable eDP
1		Disable eDP

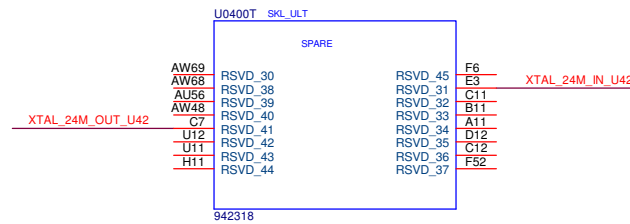
Signal Name	Description
Vss	Processor ground node
Vss_NCTF	Non-Critical To Function: These signals are for package mechanical reliability.
RSVD	Reserved: All signals that are RSVD and RSVD_NCTF must be left unconnected on the board. Intel recommends that all RSVD_TP signals have via test points.
RSVD_NCTF	
RSVD_TP	



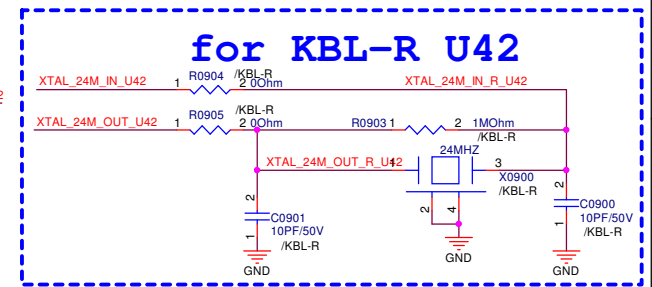
ZVM# and MSM# may need to control the VCC0P0 and VCC0P10.

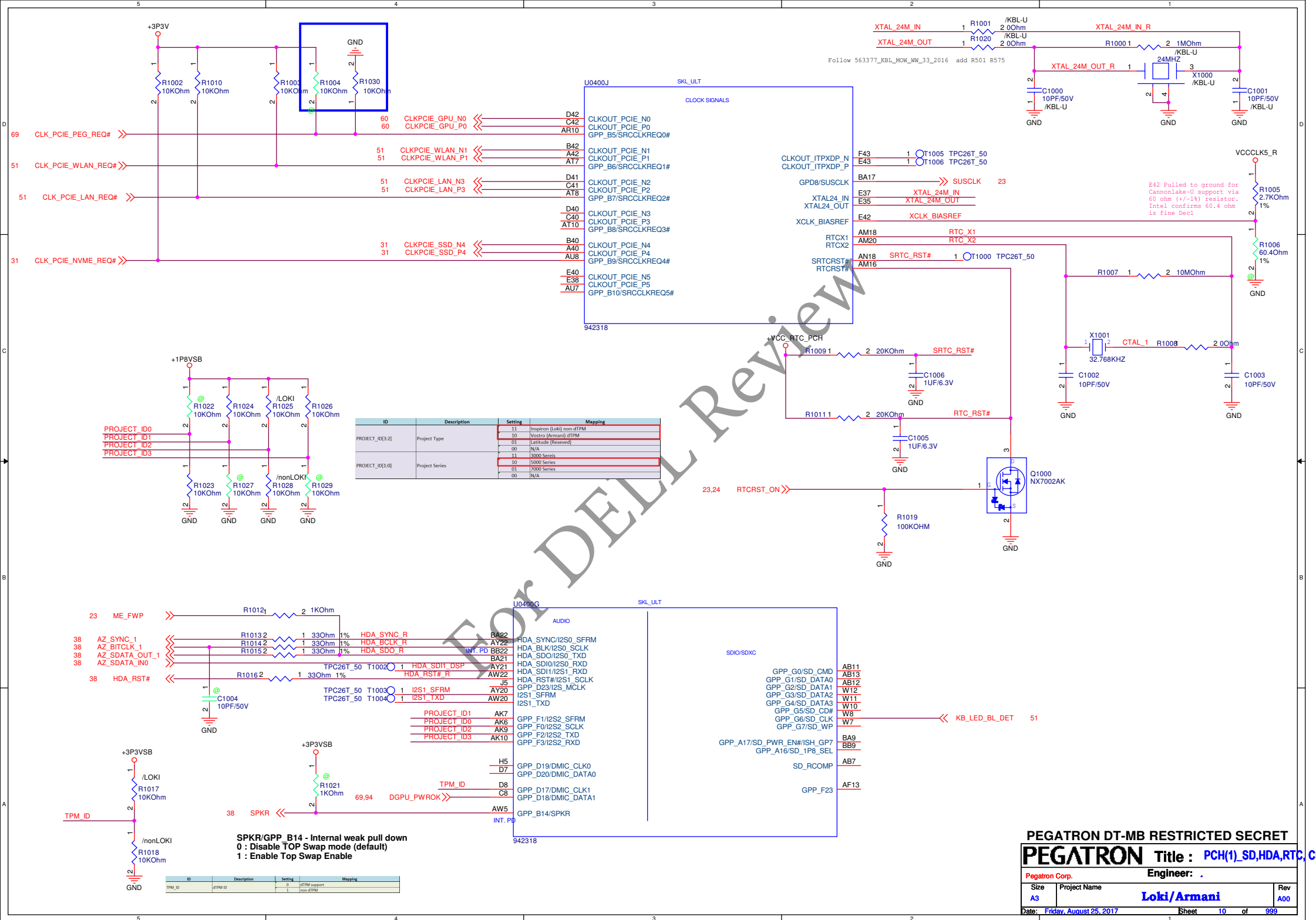
1. Ball C64 which is PROC_SELECT# needs to be pulled to VCCST for Cannonlake support via 100K ohm resistor and with no resistor populated (floating pin) for Skylake.

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	<p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none"> CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted: <ul style="list-style-type: none"> 1 = (Default) Normal Operation; No stall. 0 = Stall. CFG[1]: Reserved configuration lane. CFG[2]: PCI Express* Static x16 Lane Numbering Reversal. <ul style="list-style-type: none"> 1 = Normal operation 0 = Lane numbers reversed. CFG[3]: Reserved configuration lane. CFG[4]: eDP* enable: <ul style="list-style-type: none"> 1 = Disabled. 0 = Enabled. CFG[6:5]: PCI Express* Bifurcation <ul style="list-style-type: none"> 00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express* CFG[7]: PEG Training: <ul style="list-style-type: none"> 1 = (default) PEG Train immediately following RESET# de assertion. 0 = PEG Wait for BIOS for training. CFG[19:8]: Reserved configuration lanes. 	I	GTL	SE	All processor lines.
CFG_RCOMP	Configuration Resistance Compensation	N/A	N/A	SE	All processor lines
PROC_POPIRCOMP	POPIO Resistance Compensation	N/A	N/A	SE	Y and U-processor line
RESET#	Platform Reset pin driven by the PCH.	I	CMOS	SE	H and S-processor line
PROC_SELECT#	Processor Select: This pin is for compatibility with future platforms. It should be unconnected for KBL.			N/A	All processor lines



Ball #	Ball Names R-U42	Ball Names U22
C7	XTAL24_OUT	NC
E3	XTAL24_IN	NC
E35	NC	XTAL24_OUT
E37	NC	XTAL24_IN





GPP_C2/SMBALERT#	
0 Default	Disable ME crypto TLS
1	Enable ME crypto TLS

GPP_C5/SML0ALERT#	
0 Default	LPC (EC)
1	eSPI (EC)

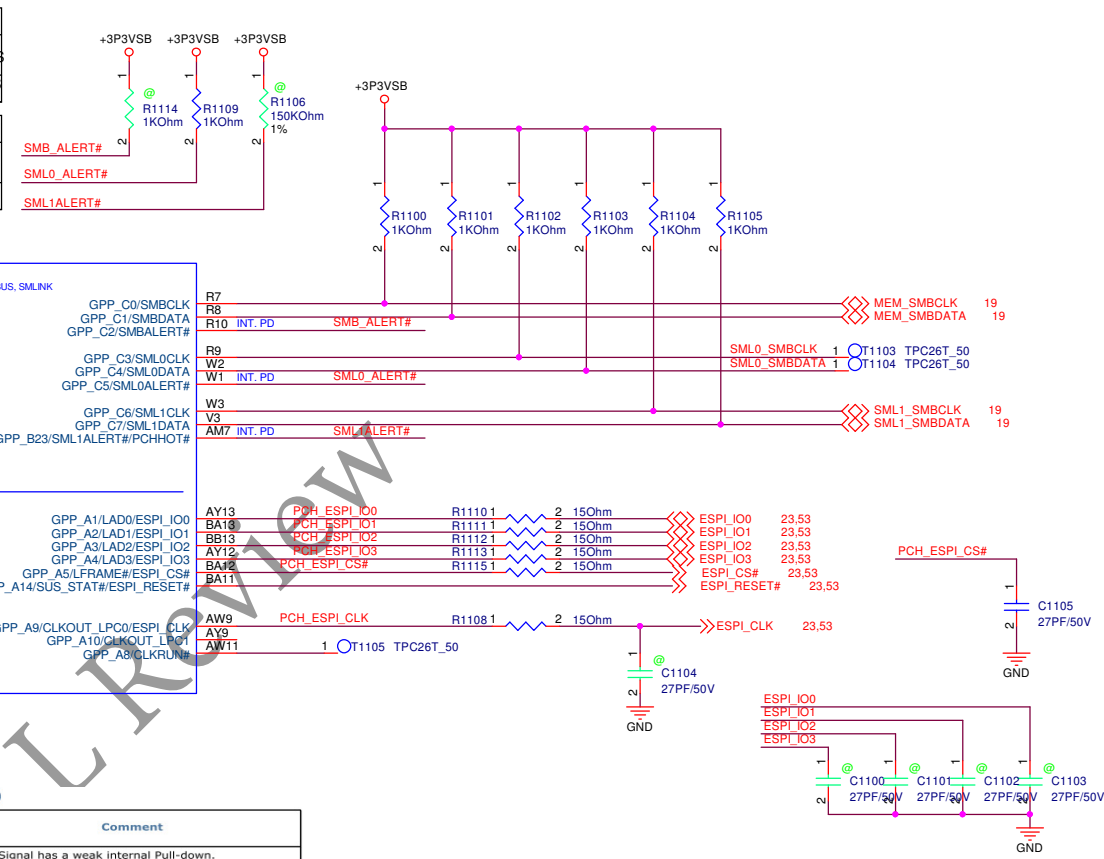


Table 9-1. Functional Strap Definitions (Sheet 2 of 3)

Signal	Usage	When Sampled	Comment
GSPI1_MOSI/ GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	<p>This Signal has a weak internal Pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6).</p> <p>Bit 6</p> <p>0 = Boot BIOS Destination 1 = SPI (Default) 2 = LPC</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal Pull-down is disabled after PLTRST# de-asserts. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. This signal is in the primary well.
SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	<p>This signal has a weak internal Pull-down.</p> <p>0 = LPC Is selected for EC. (Default) 1 = eSPI Is selected for EC.</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal Pull-down is disabled after RSMRST# de-asserts. This signal is in the primary well.
SPI0_MOSI	Reserved	Rising edge of RSMRST#	This signal has an internal Pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_MISO	Reserved	Rising edge of RSMRST#	This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SML1ALERT# / PCHHOT# / GPP_B23	Reserved	Rising edge of RSMRST#	<p>This signal has an internal Pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p> <p>Note: When used as PCHHOT#, a 150k weak board Pull-up is recommended to ensure it does not override the internal Pull-down strap sampling.</p>
SPI0_IO2	Reserved	Rising edge of RSMRST#	This signal has an internal Pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	This signal has an internal Pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

Table 9-1. Functional Strap Definitions (Sheet 1 of 3)

Signal	Usage	When Sampled	Comment
SPKR/GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	<p>The signal has a weak internal Pull-down.</p> <p>0 = Disable "Top Swap" mode. (Default) 1 = Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (See SPI Flash Programming Guide).</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal Pull-down is disabled after PLTRST# de-asserts. Software will not be able to clear the Top Swap bit until the system is rebooted. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). This signal is in the primary well.
GSPI0_MOSI/ GPP_B18	No Reboot	Rising edge of PCH_PWROK	<p>The signal has a weak internal Pull-down.</p> <p>0 = Disable "No Reboot" mode. (Default) 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal Pull-down is disabled after PLTRST# de-asserts. This signal is in the primary well.
SMBALERT# / GPP_C2	TLS Confidentiality	Rising edge of RSMRST#	<p>This signal has a weak internal Pull-down.</p> <p>0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal Pull-down is disabled after RSMRST# de-asserts. This signal is in the primary well.

Table 9-1. Functional Strap Definitions (Sheet 3 of 3)

Signal	Usage	When Sampled	Comment
HDA_SDO / I2S_TXD0	Flash Descriptor Security Override	Rising edge of PCH_PWROK	<p>This signal has a weak internal Pull-down.</p> <p>0 = Enable security measures defined in the Flash Descriptor. (Default) 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY.</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal Pull-down is disabled after PLTRST# de-asserts. Asserting HDA_SDO high on the rising edge of PCH_PWROK will also halt Intel Management Engine after Chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug. This signal is in the primary well.
DDPB_CTRLDATA/ GPP_E19	Display Port B Detected	Rising edge of PCH_PWROK	<p>This signal has a weak internal Pull-down.</p> <p>0 = Port B is not detected. (Default) 1 = Port B is detected.</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal Pull-down is disabled after PLTRST# de-asserts. This signal is in the primary well.
DDPC_CTRLDATA/ GPP_E21	Display Port C Detected	Rising edge of PCH_PWROK	<p>This signal has a weak internal Pull-down.</p> <p>0 = Port C is not detected. (Default) 1 = Port C is detected.</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal Pull-down is disabled after PLTRST# de-asserts. This signal is in the primary well.

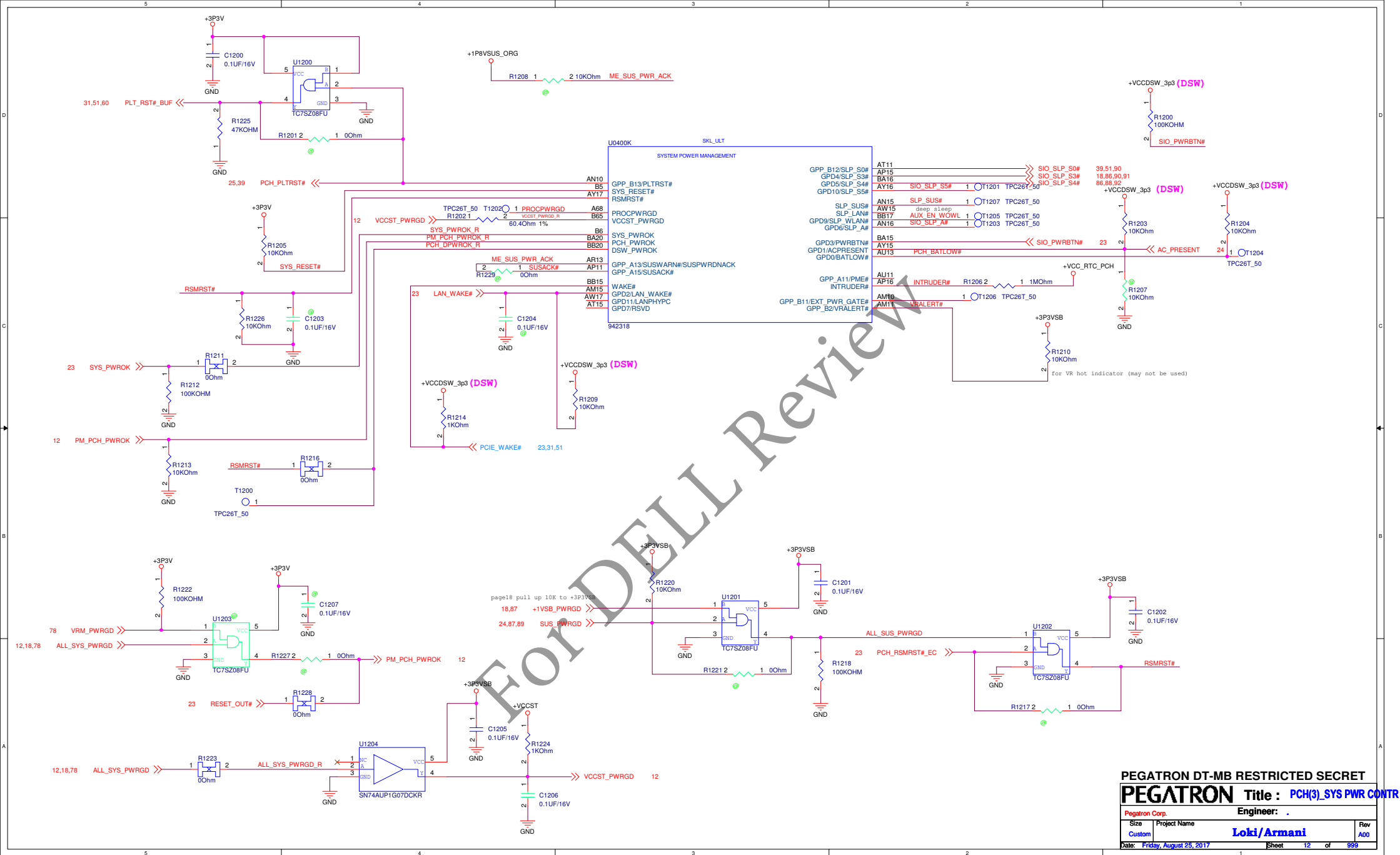
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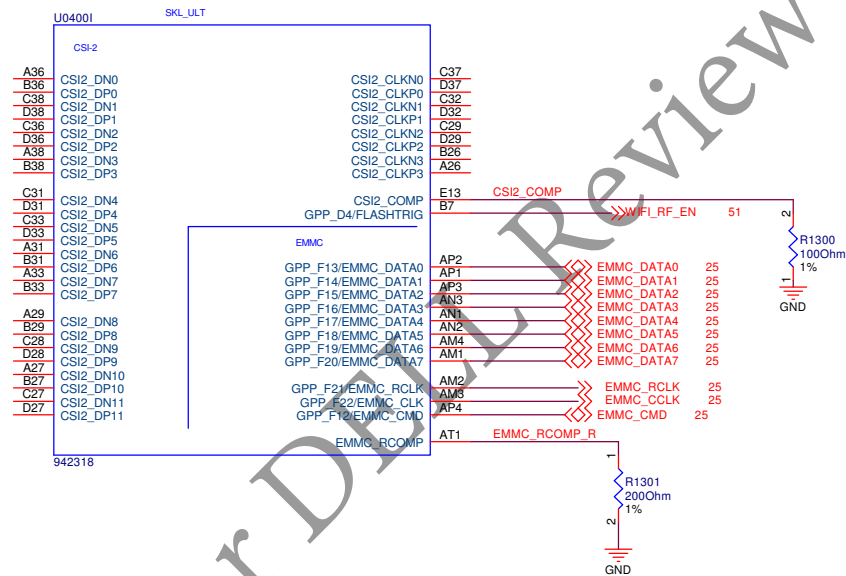
PEGATRON Title : PCH(2)_CLK,SMB,LPC,S

Pegatron Corp. Engineer: .

Size A3 Project Name Loki/Armani

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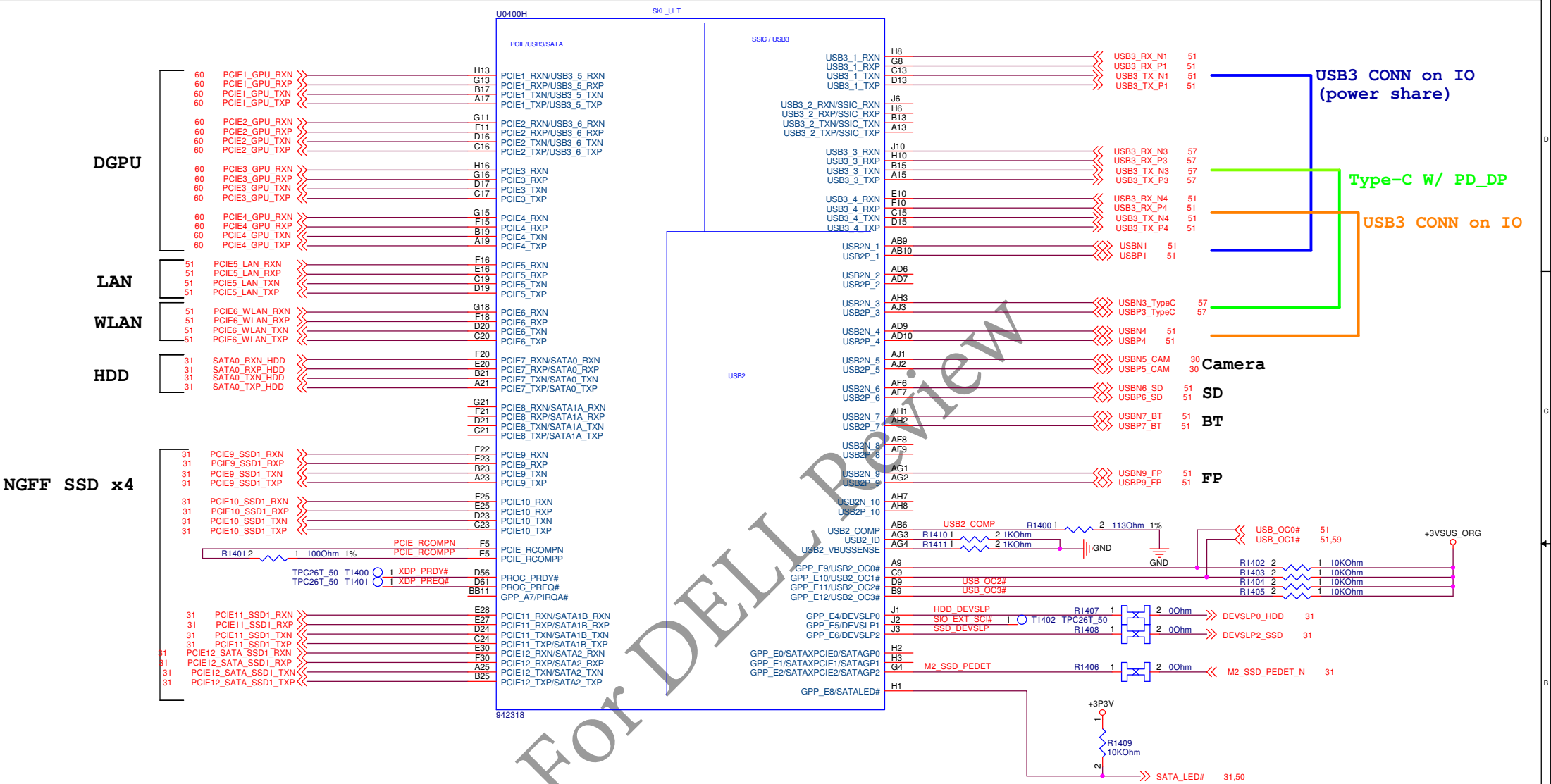
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PEGATRON Title : PCH(4)_CCI, HWID

Pegatron Corp. Engineer: .

Size A3	Project Name Loki/Armani	Rev A00
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PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH(5)_PCIE,USB

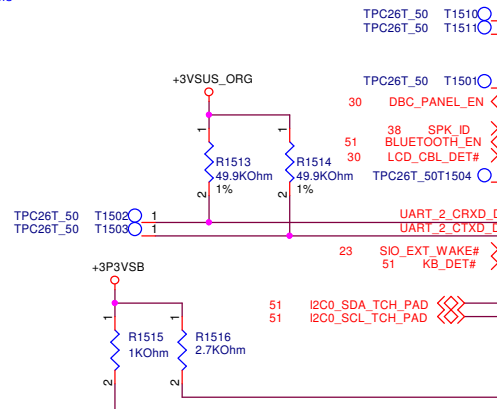
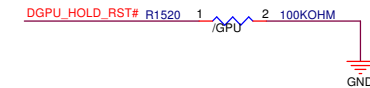
Pegatron Corp. Engineer: .

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A3	Loki/Armani	A00

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NRB_BIT
 No reboot strap
 Low: Disable (Default)
 High: Enable

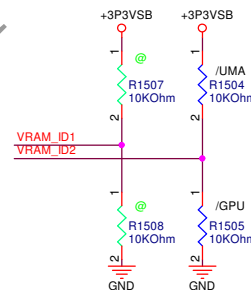
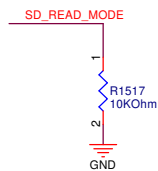


Intel KBL-U PDG : Recommended I2C Rpu value is 1 KΩ for 100 KHz / 400 KHz and 0.5 KΩ for 1 MHz.

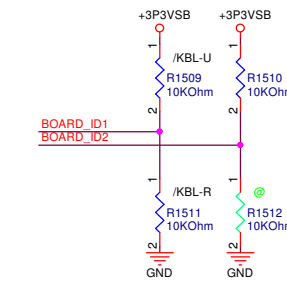
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		10	Micron
		01	Hynix
		00	Samsung
MEM_CONFIG[2:1]	On-board memory configuration for total memory size per channel	11	N/A
		10	16GB
		01	8GB
		00	4GB
MEM_CONFIG[0]	SDP/DDP Configuration	1	SDP (Single Die per Package)
		0	DDP (Dual Die per Package)

GPP_B22 : Boot BIOS Strap
 Sampled on rising edge of PWROK.

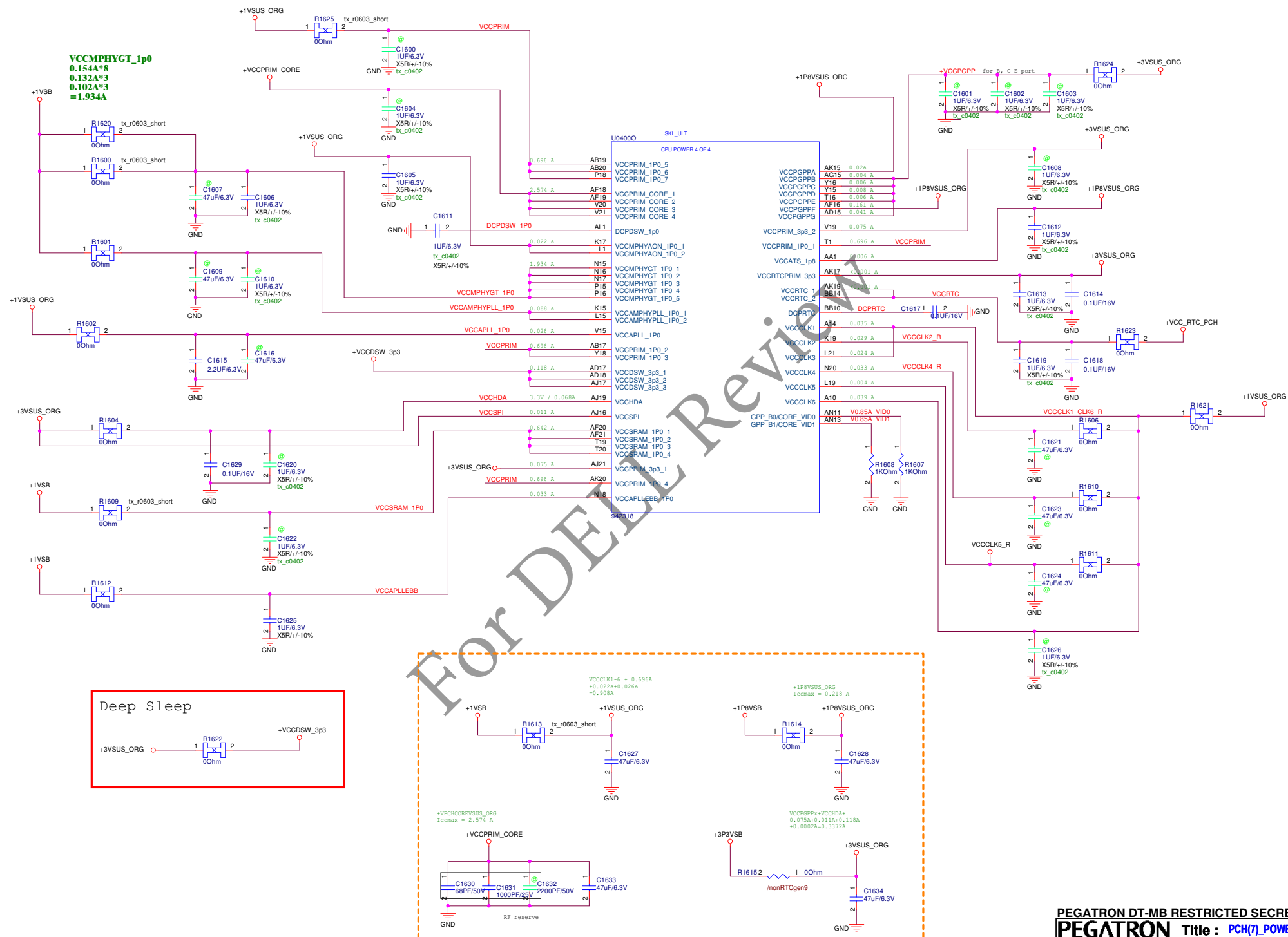
Boot BIOS Strap	
GPP_B22	Boot BIOS Location
1	LPC
0	SPI (PCH)



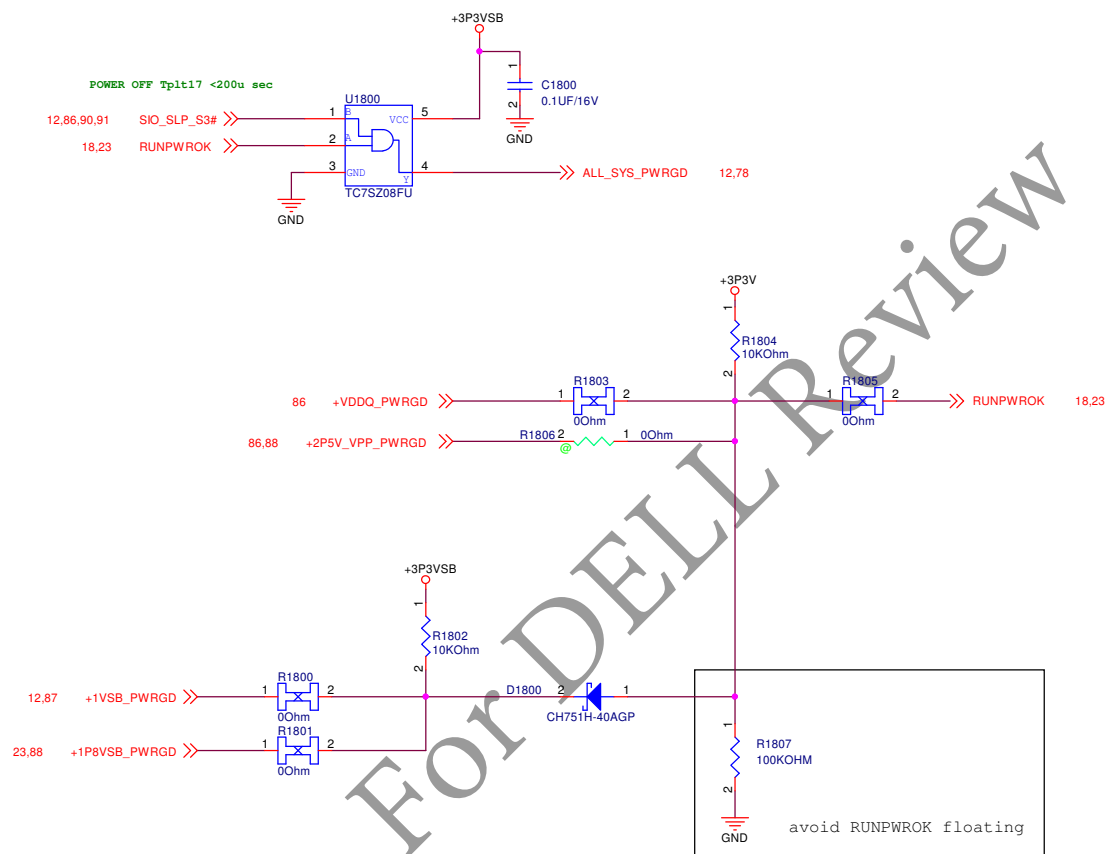
ID	Description	Setting	Mapping
VRAM_ID[2:1]	dGPU VRAM size	11	UMA Board
		10	N/A
		01	DIS Board with 4GB VRAM
		00	DIS Board with 2GB VRAM



ID	Description	Setting	Mapping
BOARD_ID[2:1]	Board SKU ID	11	KBL-U
		10	KBL-R
		01	N/A
		00	SKL-U



POWER GOOD DETECTOR



PEGATRON DT-MB RESTRICTED SECRET

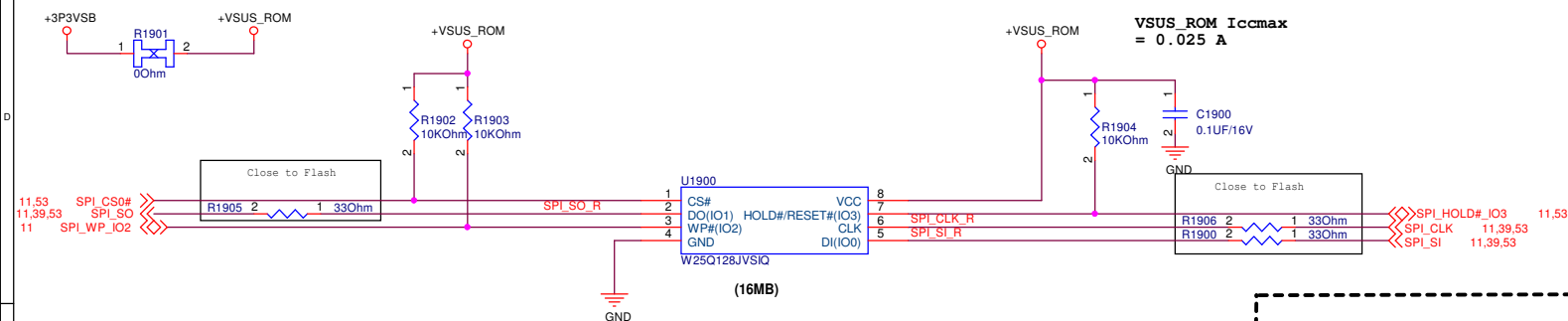
PEGATRON Title : **PWRGD DETECT**

Pegatron Corp. **Engineer:** .

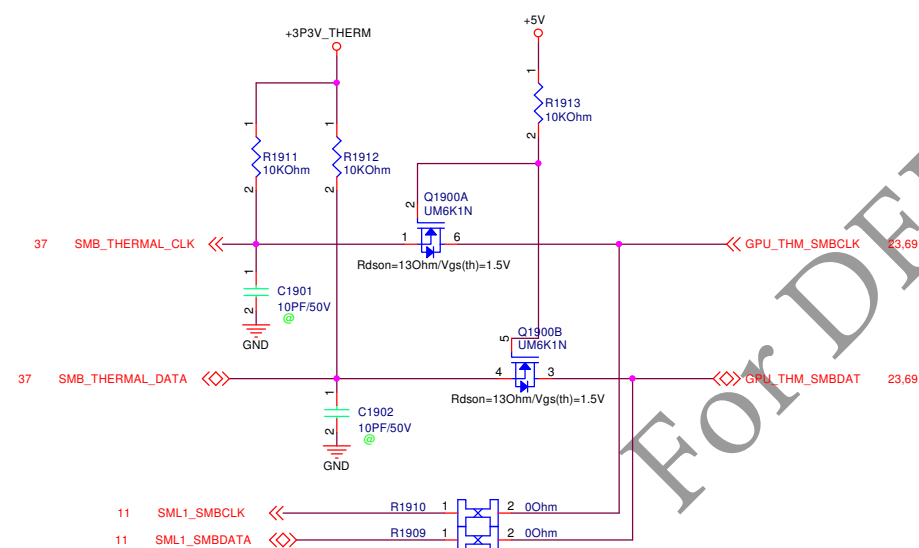
Size A3	Project Name Loki/Armani	Rev A00
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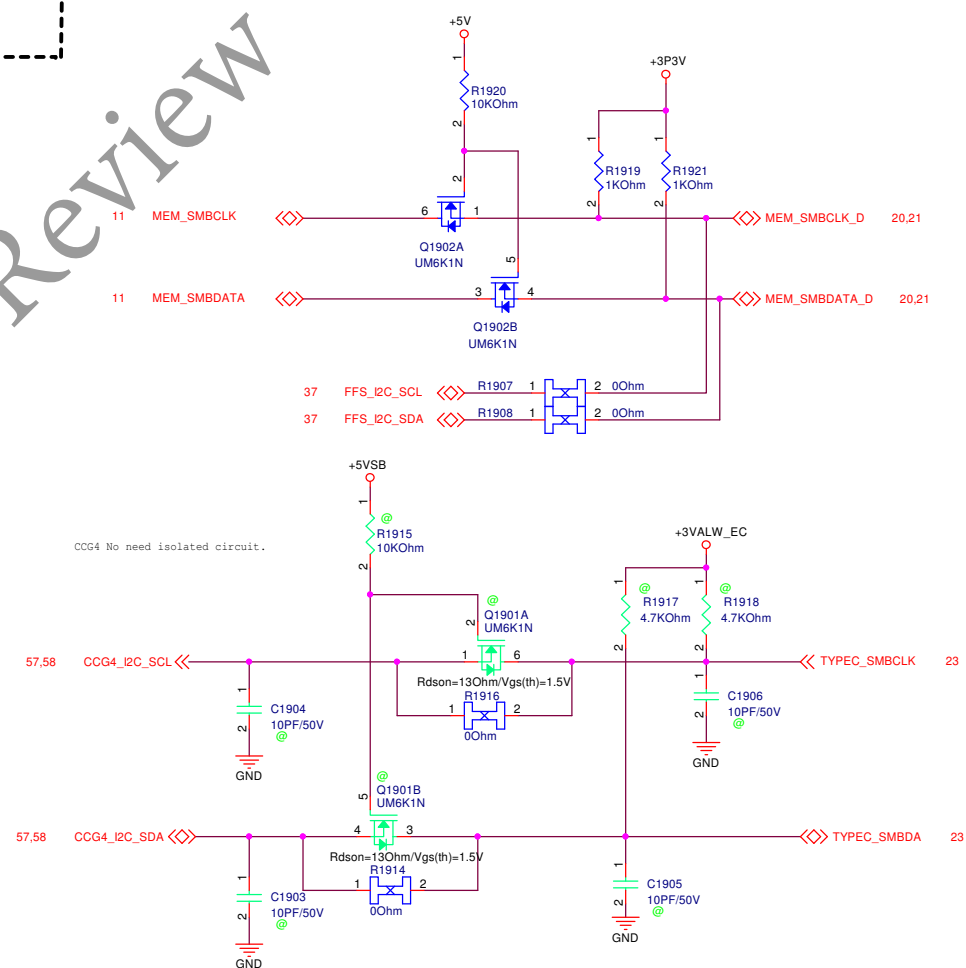
SPI ROM (Quad I/O Supported)



SM BUS



PCH side pull high +3P3VSB 1K



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SPI ROM & SM BUS

Pegatron Corp. **Engineer:** .

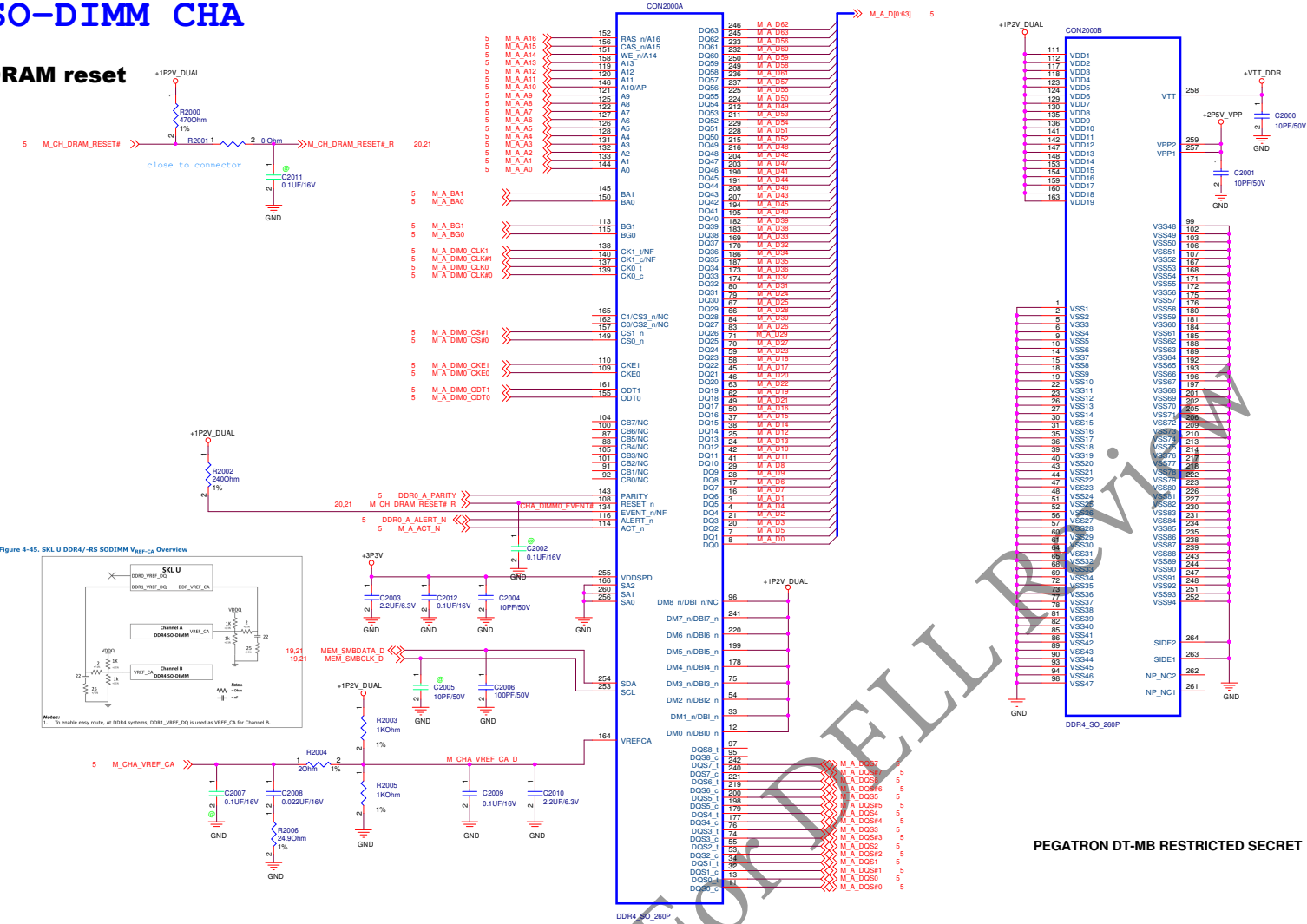
Size	Project Name	Rev
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A3	Loki/Armani	A00
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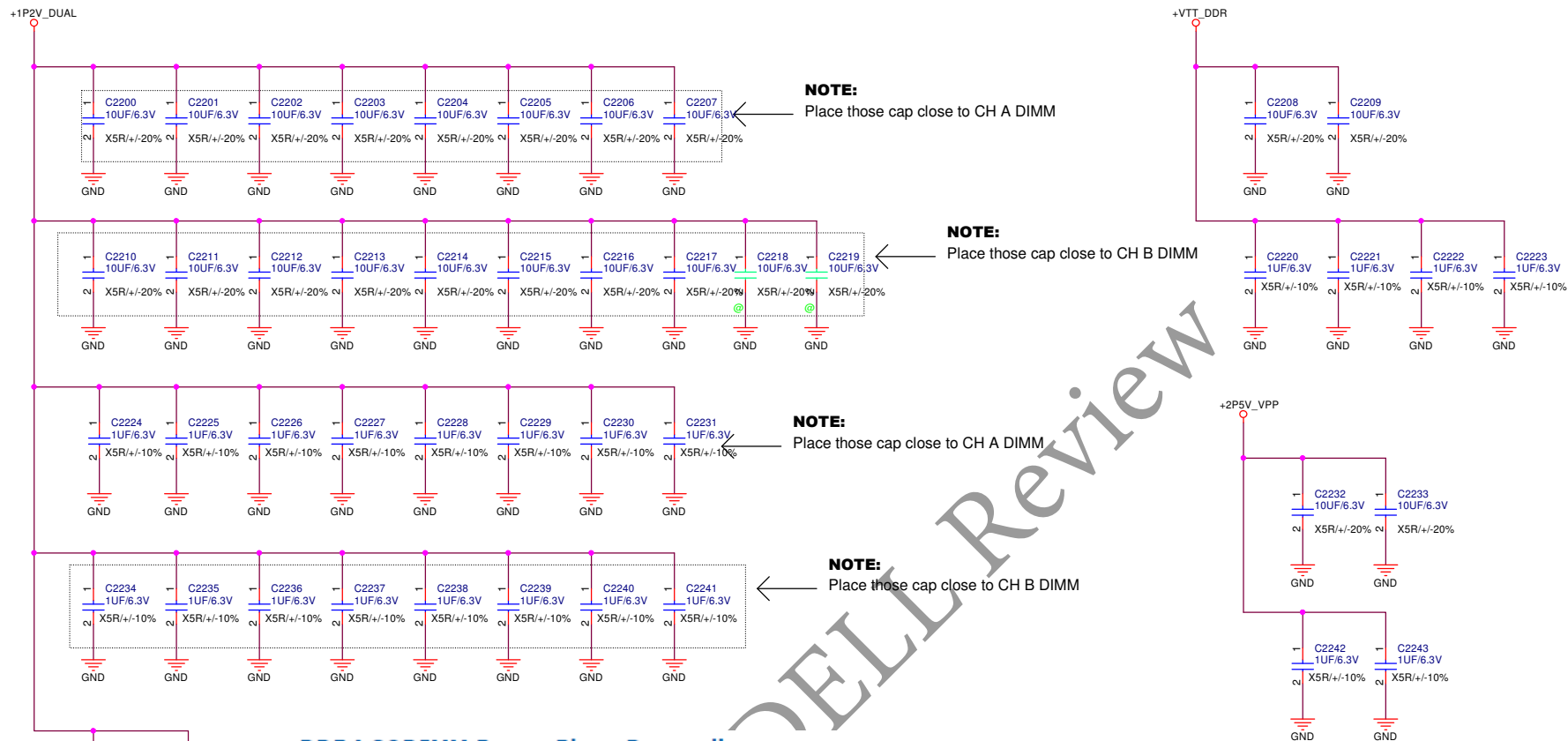
Date: Friday, August 25, 2017 Sheet 19 of 999

SO-DIMM CHA

DRAM reset

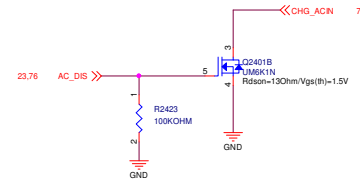
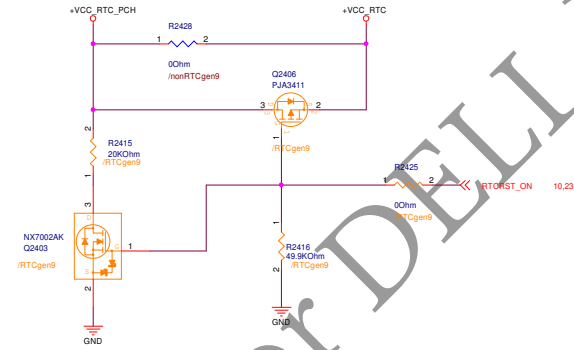
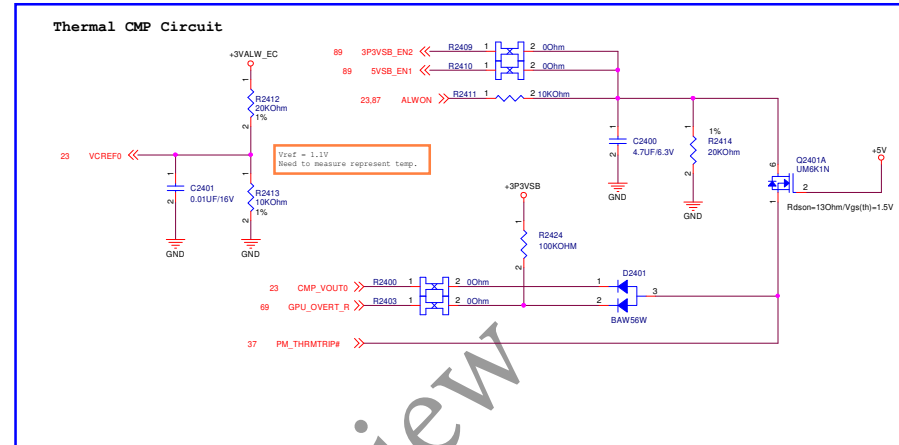
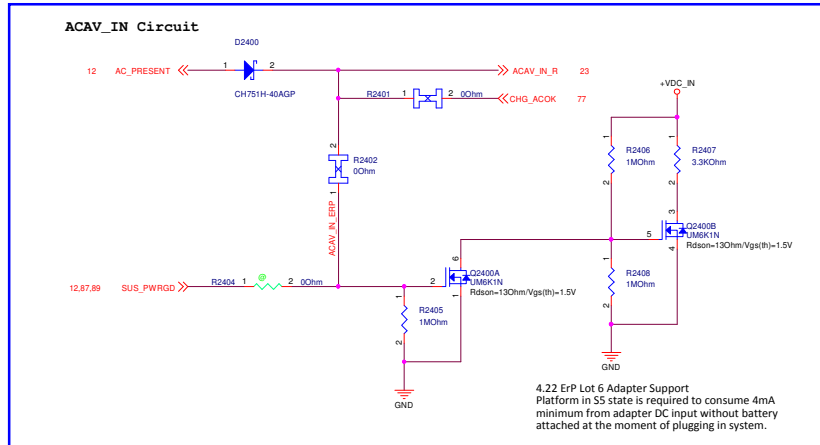


PEGATRON DT-MB RESTRICTED SECRET

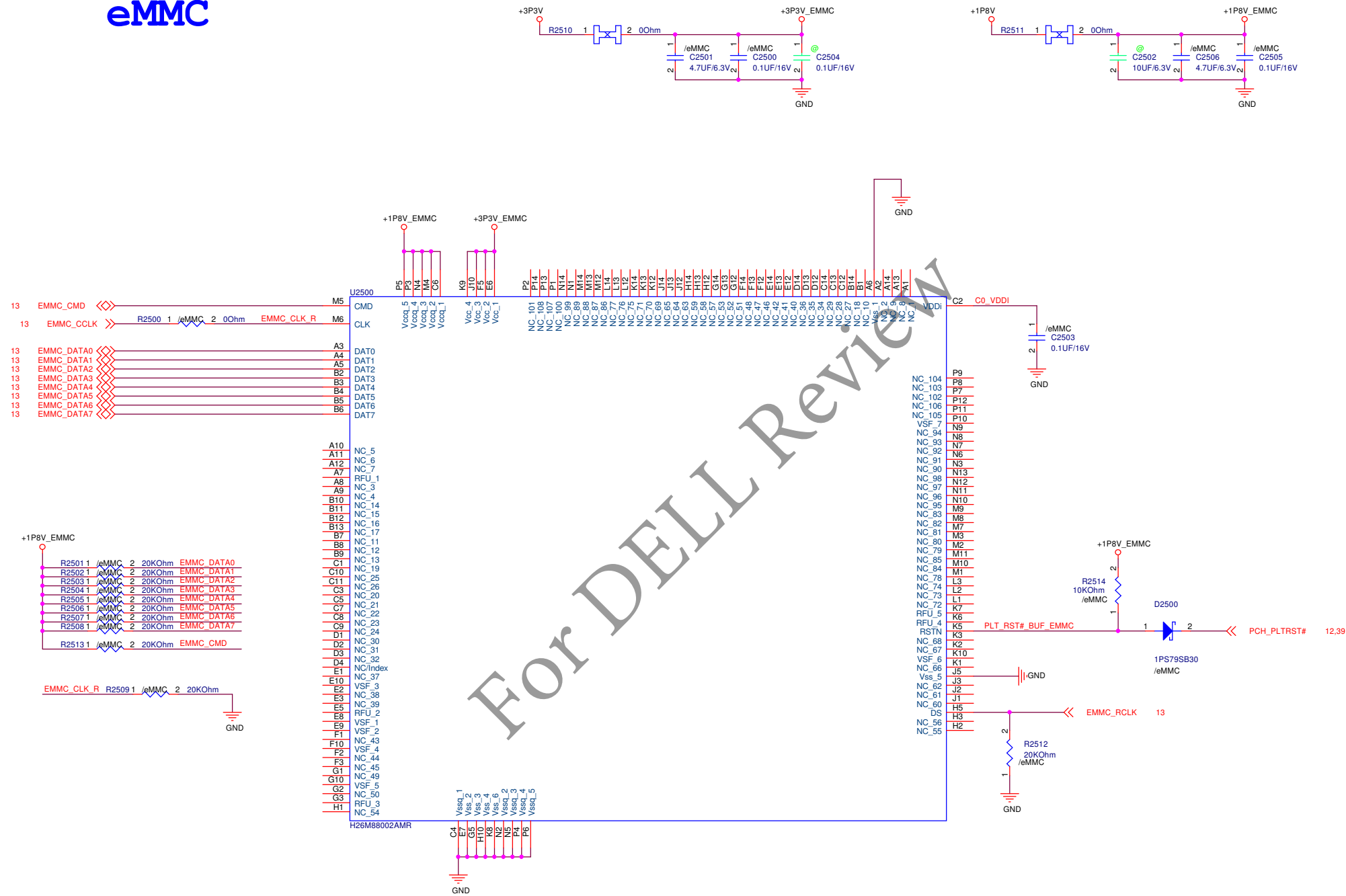


DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)	Note
DDR4 2 Channels SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10 μ F (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1 μ F (0402)	
		1 placeholder	1x 330 μ F (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10 μ F (0603)	
		Placeholder	1x 10 μ F (0603)	
		Place these caps on the VTT plane close to SODIMM	4x 1 μ F (0402)	
	VPP	DRAM Side	2x 10 μ F (0603)	
		DRAM Side	2x 1 μ F (0402)	
	VDDSPD	Place close to DIMM	1x 0.1 μ F (0402)	
		Place close to DIMM	1x 22 μ F (0402)	



eMMC



Intel PDG R2.0 : If the interface is used, external pull-up resistors of 20 KΩ are required on the Data lines. A pull-down resistor of 20 KΩ is recommended on the Clock lines.

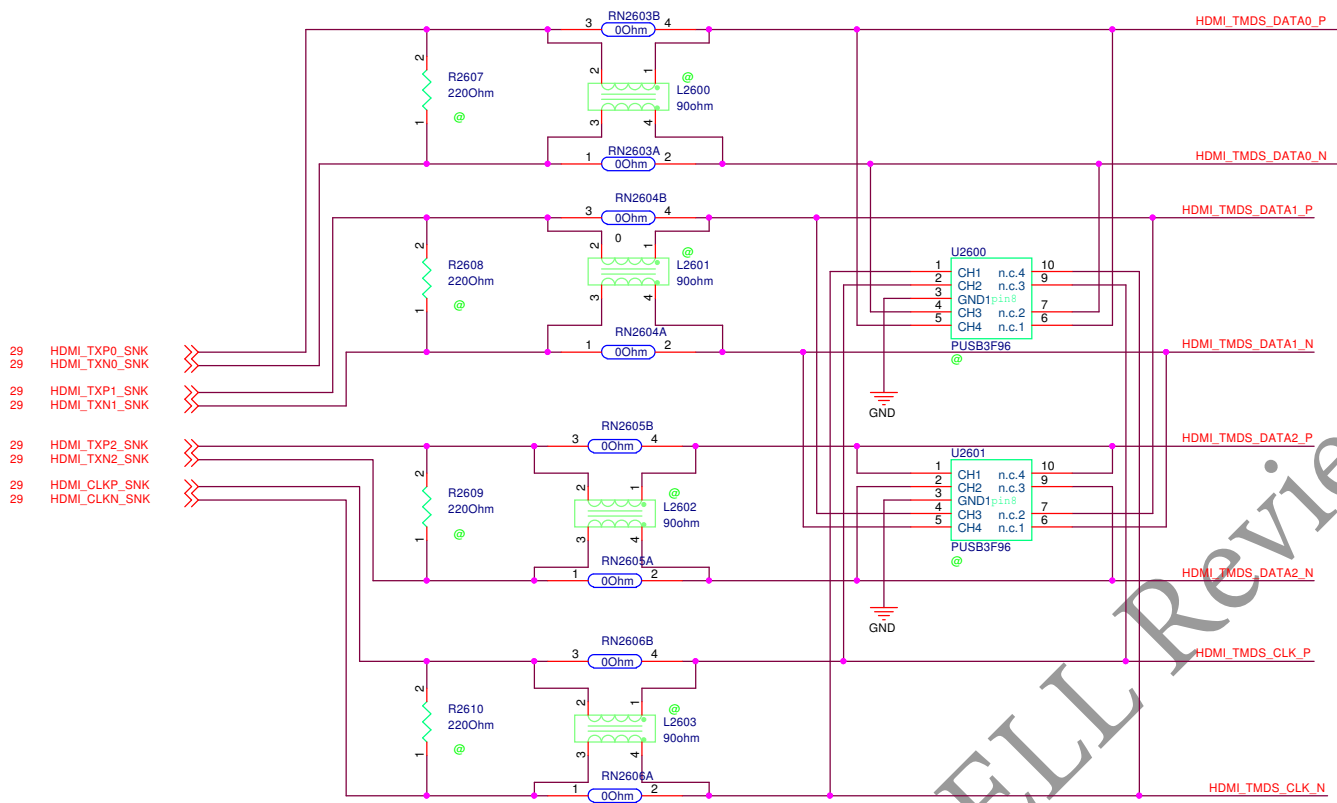
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **EMMC**

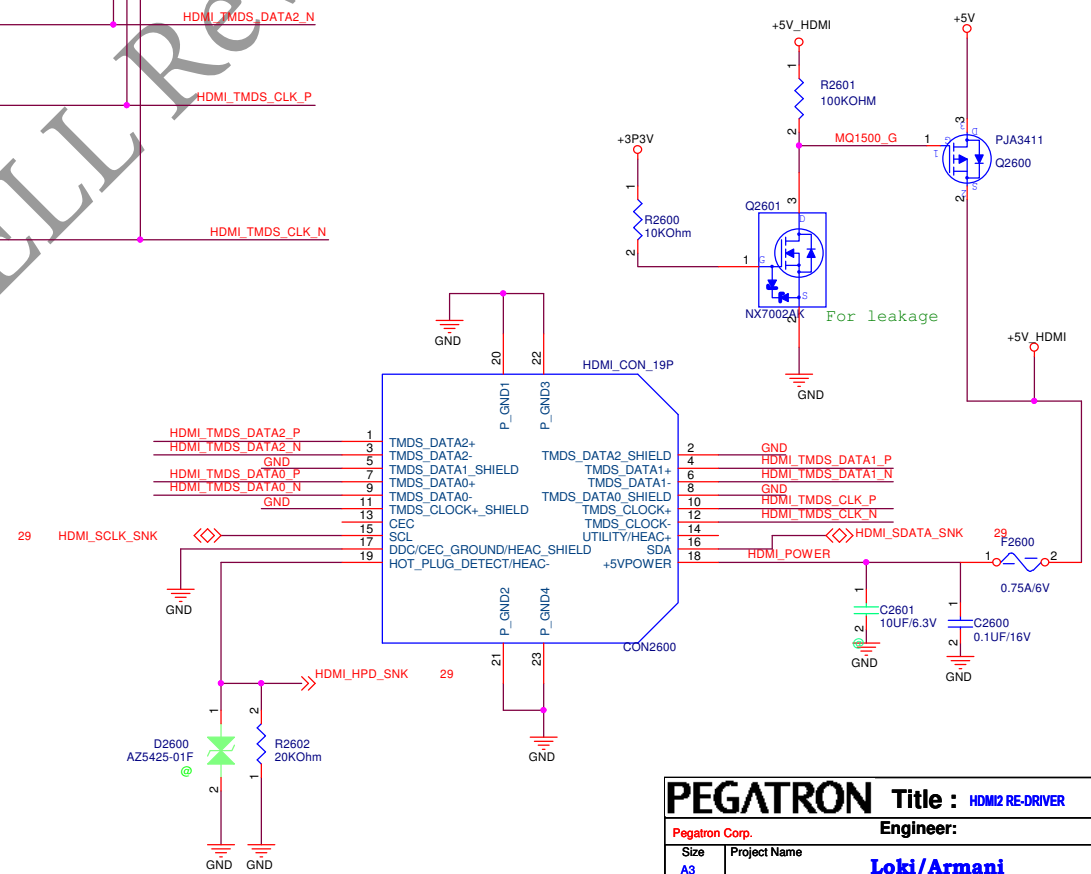
Pegatron Corp. Engineer: .

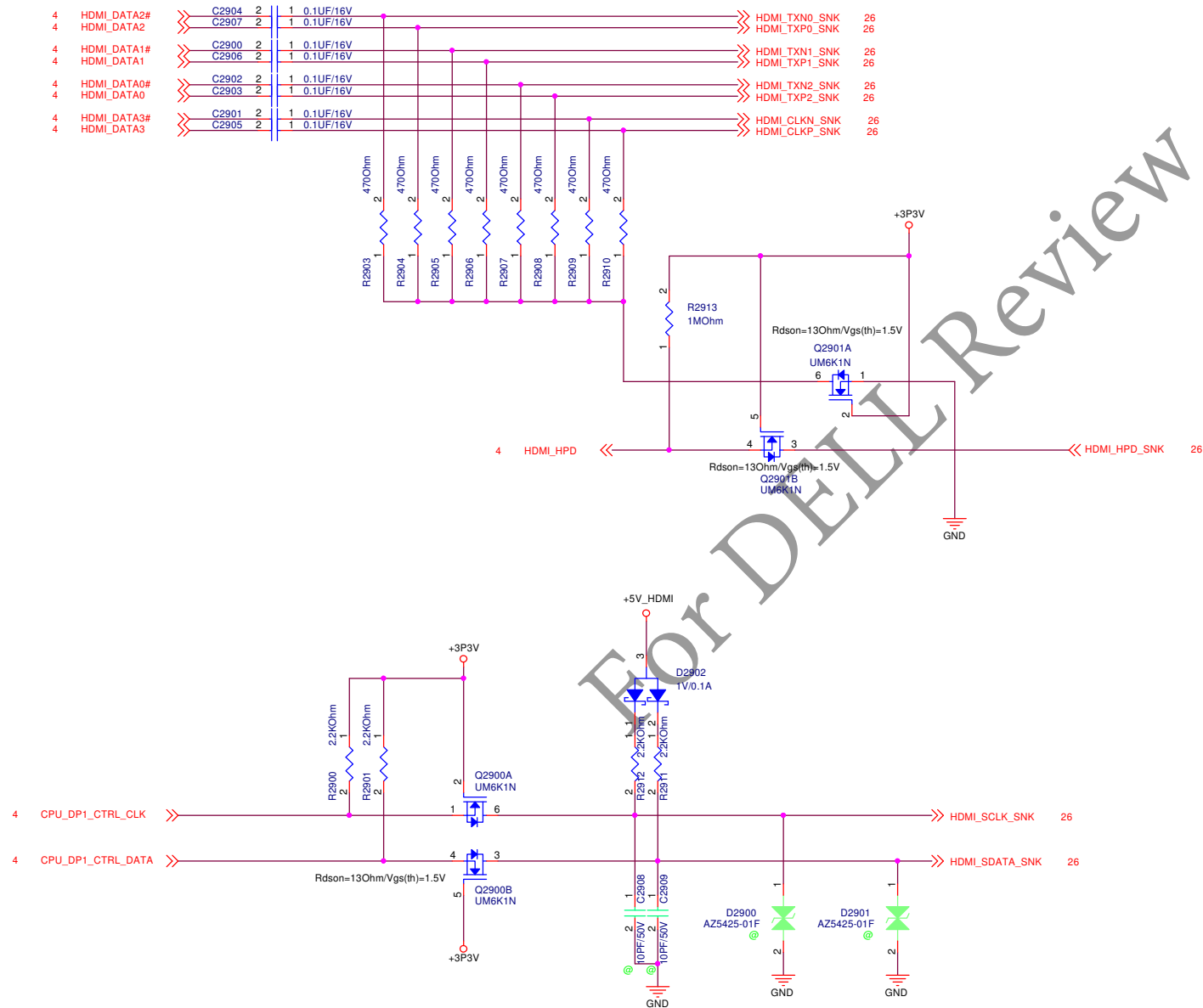
Size	Project Name	Rev
A3	Loki/Armani	A00

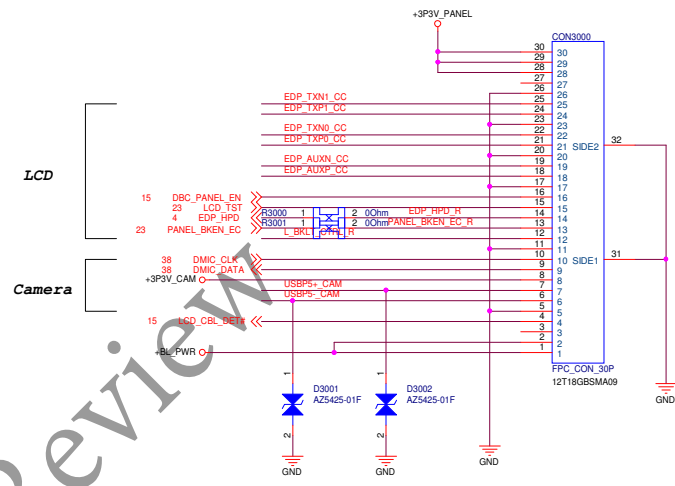
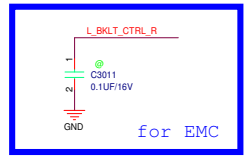
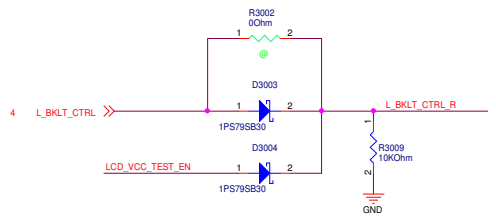
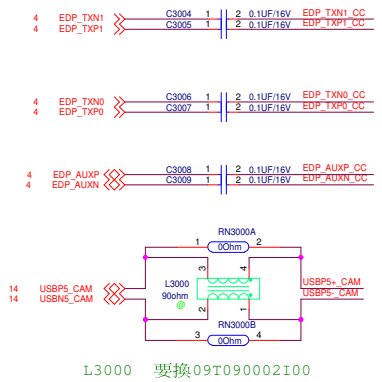
Date: Friday, August 25, 2017 Sheet 25 of 999



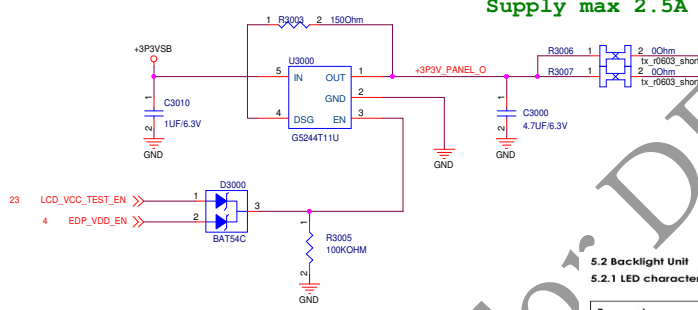
HDMI connector		
pin1	TMDS Data2+	
pin2	TMDS Data2 Shield(GND)	
pin3	TMDS Data2 -	
pin4	TMDS Data1+	
pin5	TMDS Data1 Shield(GND)	
pin6	TMDS Data1 -	
pin7	TMDS Data0+	
pin8	TMDS Data0 Shield(GND)	
pin9	TMDS Data0 -	
pin10	TMDS Clock+	
pin11	TMDS Clock Shield(GND)	
pin12	TMDS Clock -	
pin13	CEC	
pin14	Reserved {N.C. on device }	
pin15	SCL	
pin16	SDA	
pin17	DDC/CEC Ground	
pin18	+5V Power	
pin19	Hot Plug Detect	





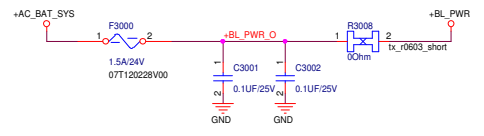


Panel power

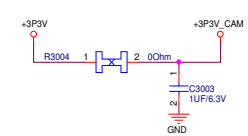


Supply max 2.5A

Backlight power



Camera power



Symbol	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	2.4	[Watt]	Note 1
IDD	IDD Current	-	-	800	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

5.2 Backlight Unit
5.2.1 LED characteristics

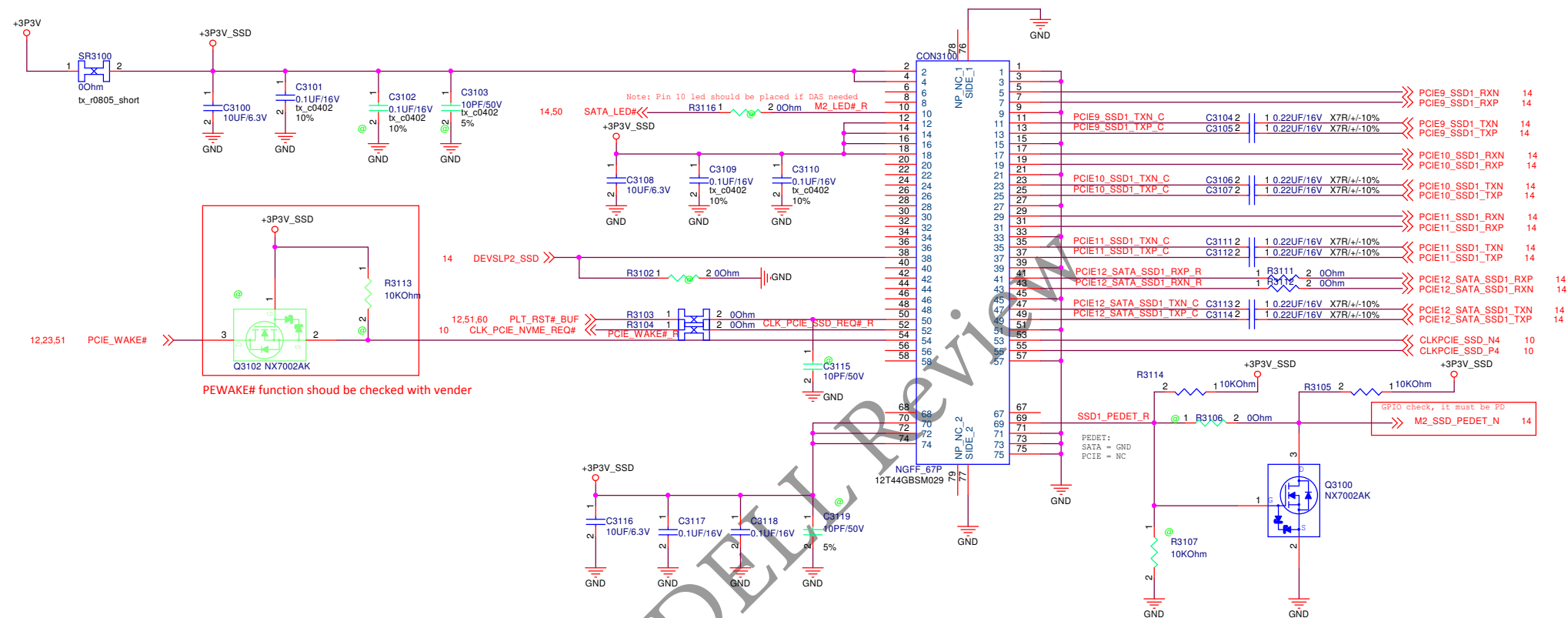
Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	5.6	[Watt]	(Ta=25°C), Note 1 Vin=12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25°C), Note 2 Ib=23 mA

Note 1: Calculator value for reference $P_{LED} = V_F$ (Normal Distribution) * IF (Normal Distribution) / Efficiency
Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	10	12.0	21.0	[Volt]	

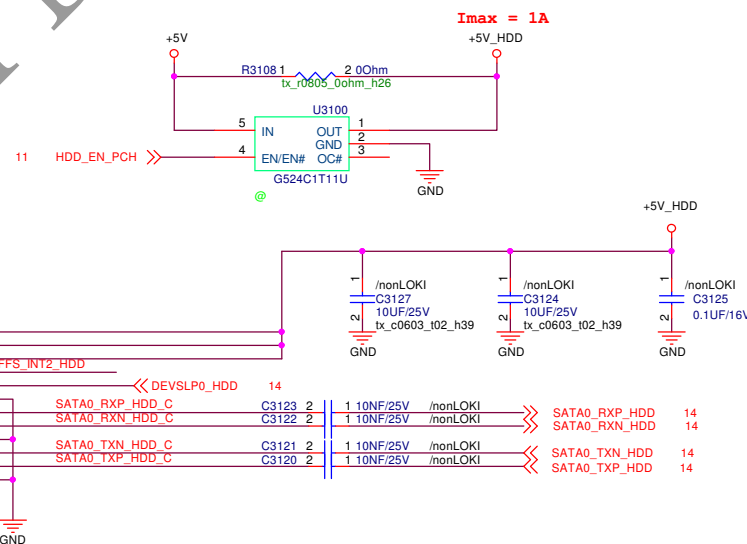
M.2 KEY-M 2280 SSD #1 (SATA+PCIE X4)



HDD

NOTE:

- 1.Free Fall Sensor是否使用客人建議用料(closed)/FFS 是否有支援/ HDD 是否有內部PU
2.M17有要求直接至Connector Pin11, 但是實際Armani卻接至Pin 12 (closed)
3.FFS Int2 need should be pull up to 3.3V, 但是實際Armani Pull 5V, 而已Pull #電阻沒上件 (Closed)
(FFS Int2 high : Free Fall detect : Low : Normal)
4.DEVSUP1 H/L active check (H detect) : GPIO check



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **M.2 2280 SSD/ HDD**

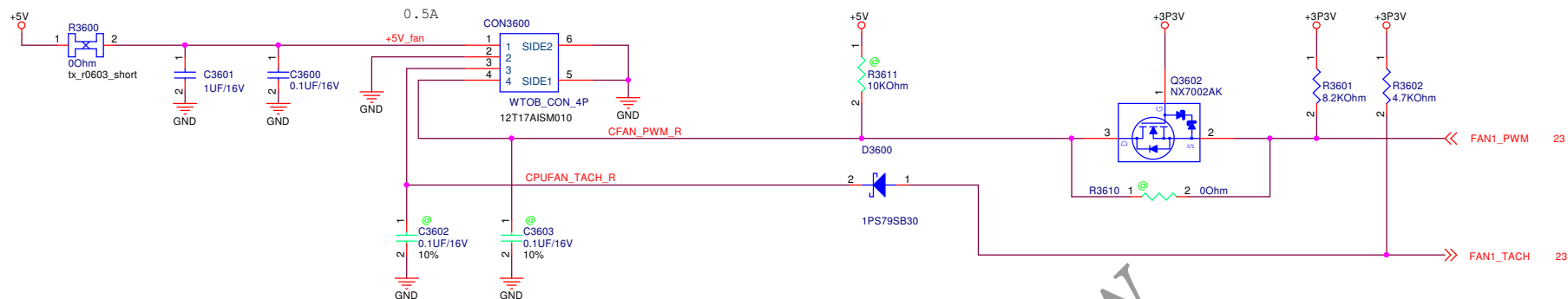
Pegatron Corp. **Engineer:** .

Size	Project Name	Rev
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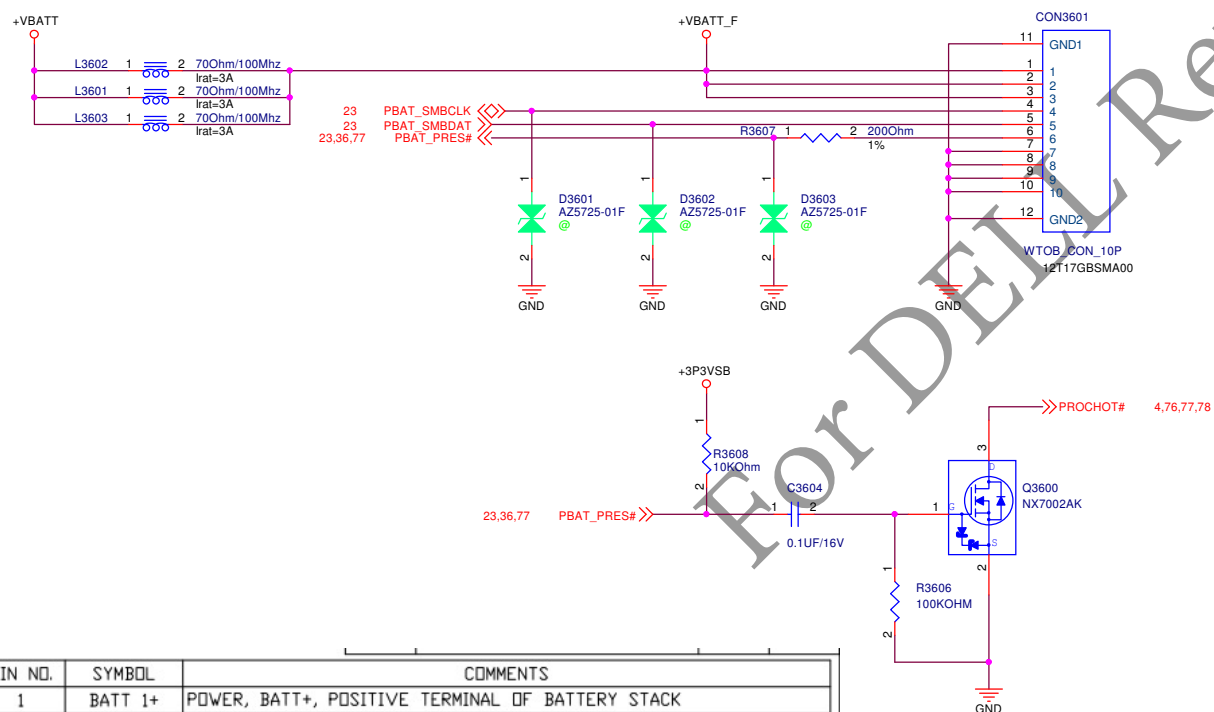
A3	Loki/Armani	A00
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Date: Friday, August 25, 2017 Sheet 31 of 999

FAN CONNECTOR

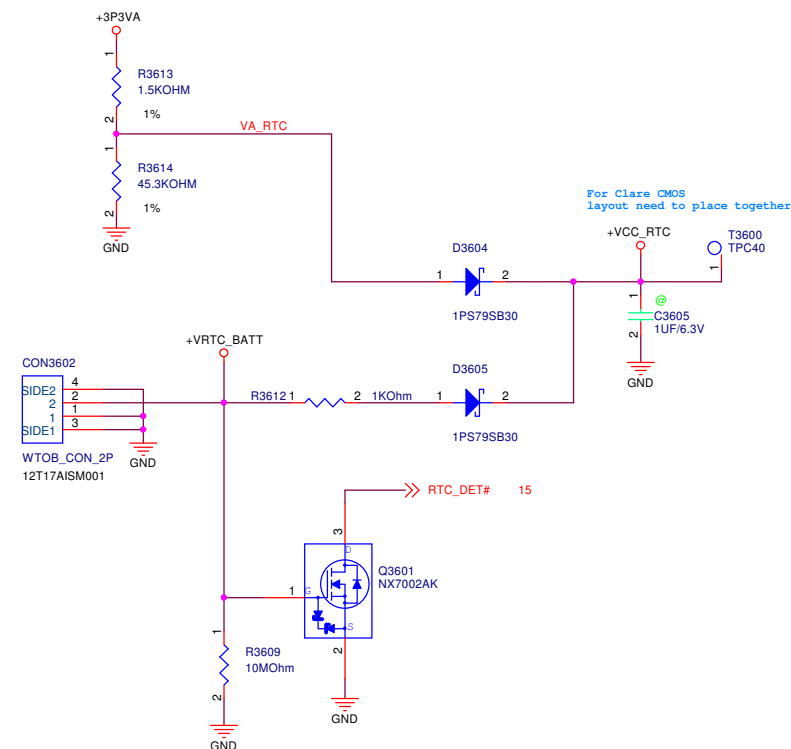


Battery CONNECTOR



PIN NO.	SYMBOL	COMMENTS
1	BATT 1+	POWER, BATT+, POSITIVE TERMINAL OF BATTERY STACK
2	BATT 2+	POWER, BATT+, POSITIVE TERMINAL OF BATTERY STACK
3	BATT 3+	POWER, BATT+, POSITIVE TERMINAL OF BATTERY STACK
4	CLK_SMB	SYSTEM MANAGEMENT BUS CLOCK
5	DAT_SMB	SYSTEM MANAGEMENT BUS CLOCK
6	BATT_PRS	BATTERY PRESENT (THIS IS TIED TO GROUND ON THE BATTERY PACK)
7	SYS_PRES	SYSTEM PRESENT (THIS IS TIED TO GROUND ON THE SYSTEM SIDE)
8	GND1	POWER, BATT-, NEGATIVE TERMINAL OF BATTERY STACK
9	GND2	POWER, BATT-, NEGATIVE TERMINAL OF BATTERY STACK
10	GND3	POWER, BATT-, NEGATIVE TERMINAL OF BATTERY STACK

RTC CONNECTOR



PEGATRON DT-MB RESTRICTED SECRET

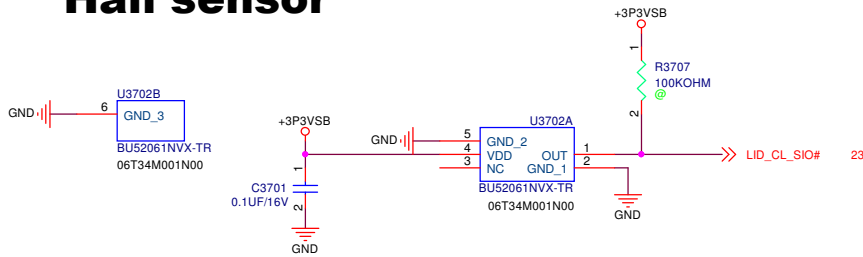
PEGATRON Title : Battery & FANConn

Pegatron Corp. **Engineer:** .

Size A3	Project Name Loki/Armani	Rev A00
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Date: Friday, August 25, 2017 Sheet 36 of 999

Hall sensor

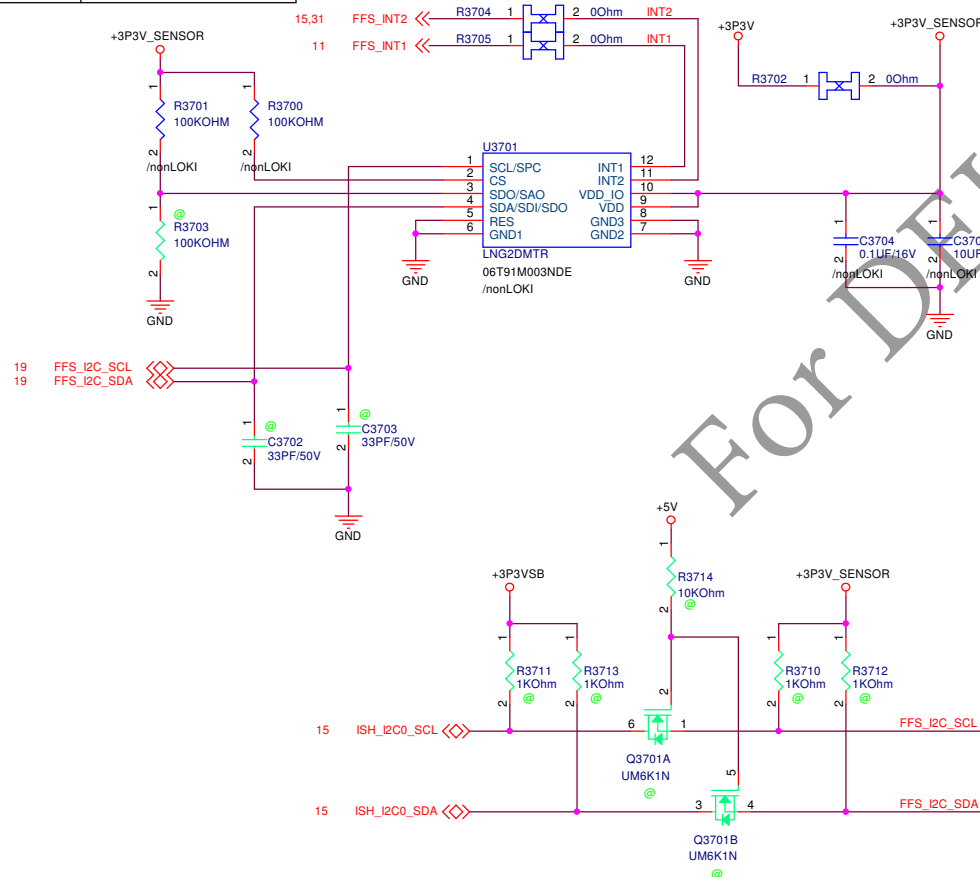


Free fall sensor

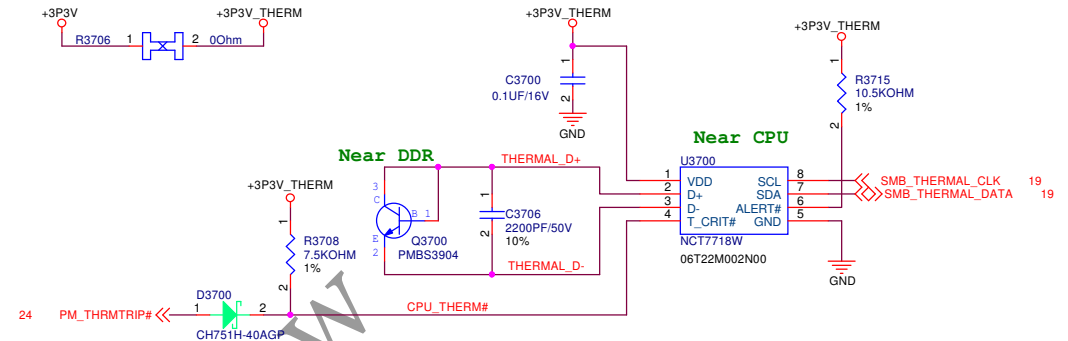
Slave address select

SA0	address
1	0101001b
0	0101000b

Default setting



Thermal sensor

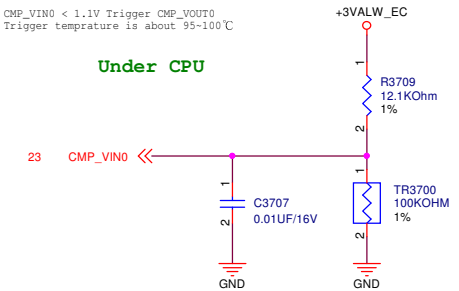


Thermistor Table

60	22.621
65	18.692
70	15.525
75	12.947
80	10.849
85	9.129
90	7.713
95	6.546
100	5.572
105	4.764
110	4.087
115	3.518
120	3.040
125	2.634

CMP_VIN0 < 1.1V Trigger CMP_VOUT0
Trigger temperature is about 95~100°C

Under CPU



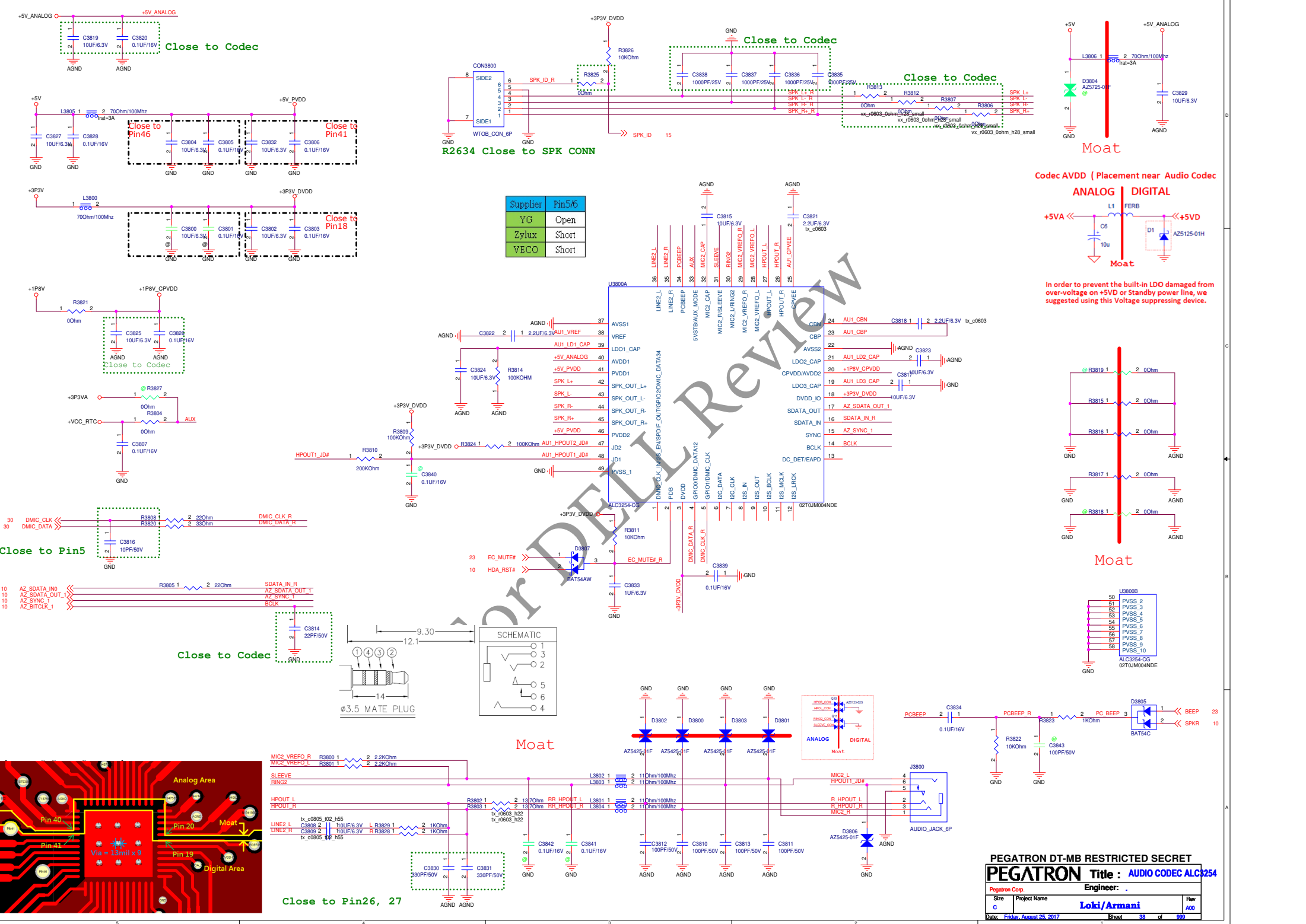
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : Sensor

Pegatron Corp. Engineer: .

Size A3 Project Name Loki/Armani Rev A00

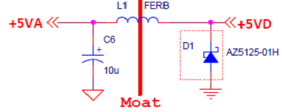
Date: Friday, August 25, 2017 Sheet 37 of 999



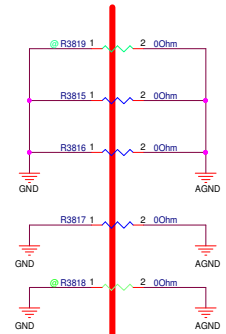
Supplier	Pin5/6
YG	Open
Zylux	Short
VECO	Short

Codec AVDD (Placement near Audio Codec

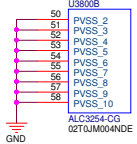
ANALOG | DIGITAL



In order to prevent the built-in LDO damaged from over-voltage on +5VD or Standby power line, we suggested using this Voltage suppressing device.



Moat



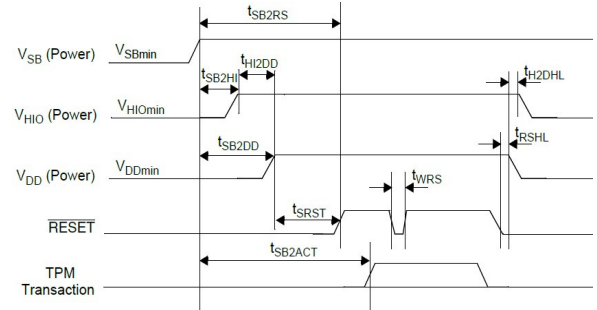
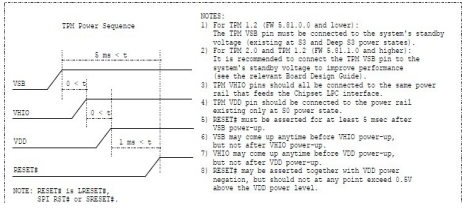
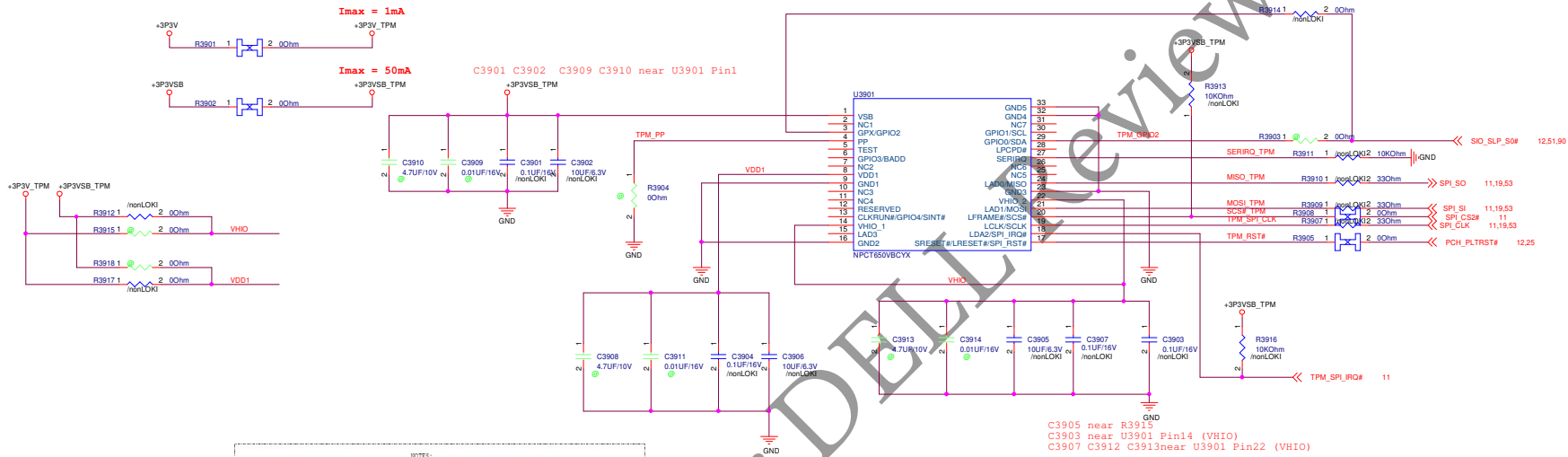
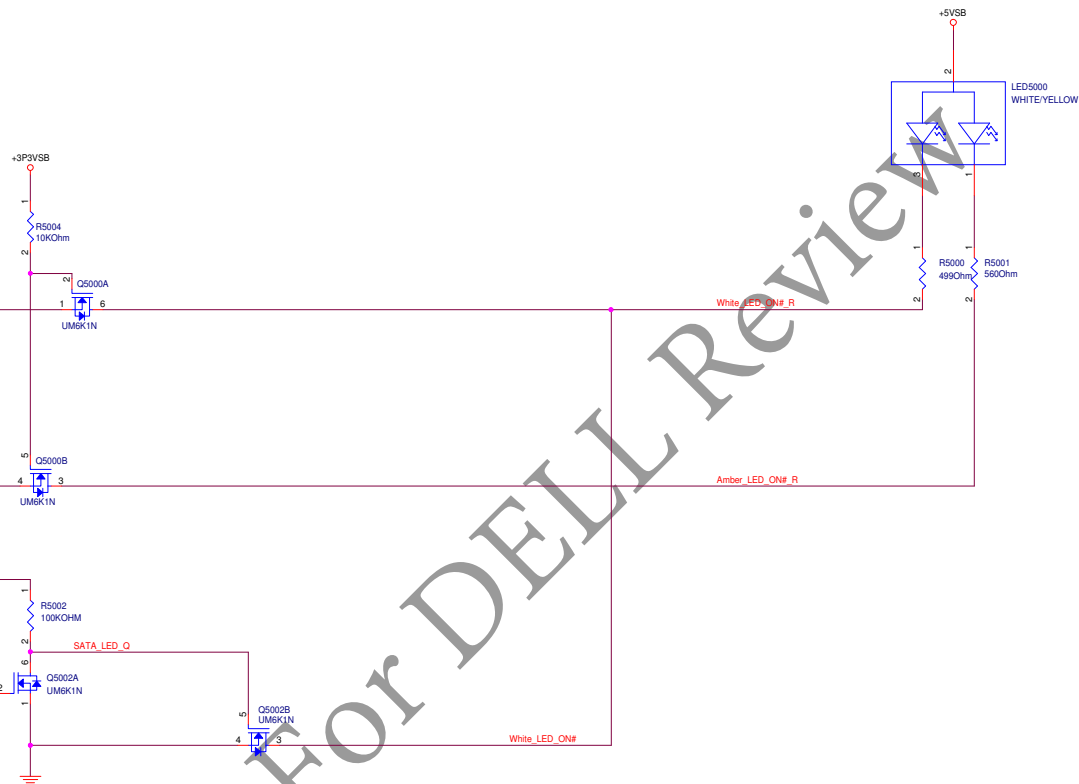


Figure 6. Reset Timing Diagram

White LED to show full charge.
Hot key can change this LED to HDD
active but need the additional GPIO
from EC(MASK_SATA_LED#)
Set EC GPIO to open drain.

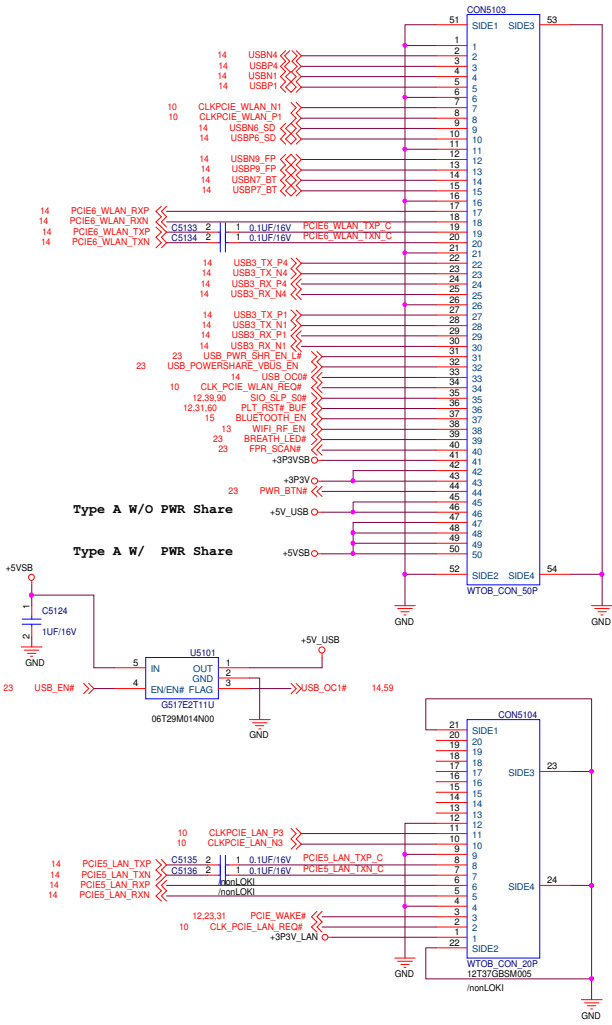
Charging LED indicate.
Set EC GPIO to open drain.

23 MASK_SATA_LED# >>>
14.31 SATA_LED# >>>
From SATA/H.2

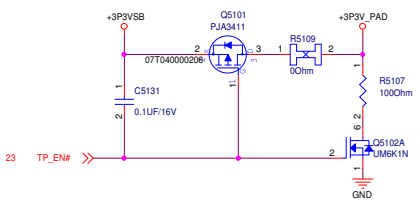


IO board Connector

Coax CONNECTOR 50 PIN

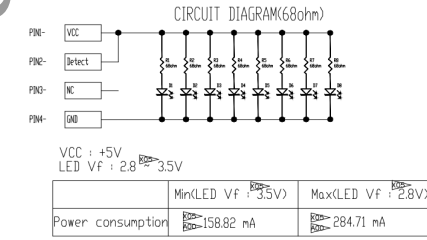
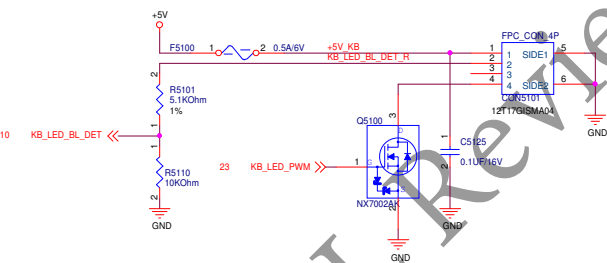


FFC CONNECTOR 12 PIN (for 14" LAN only)

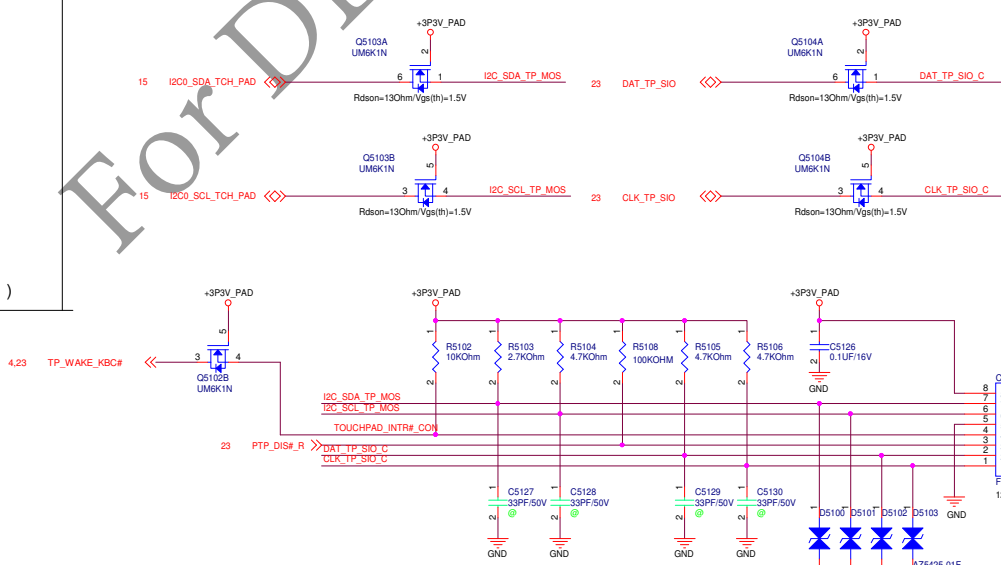


KB Conn

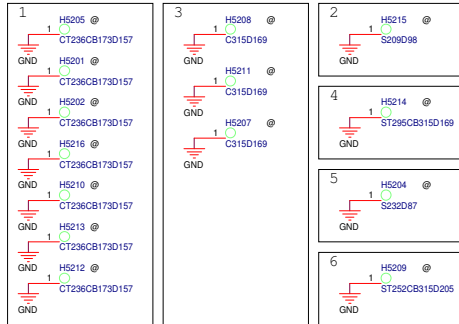
KB BL Conn



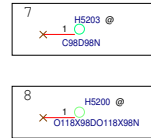
Click PAD Connector



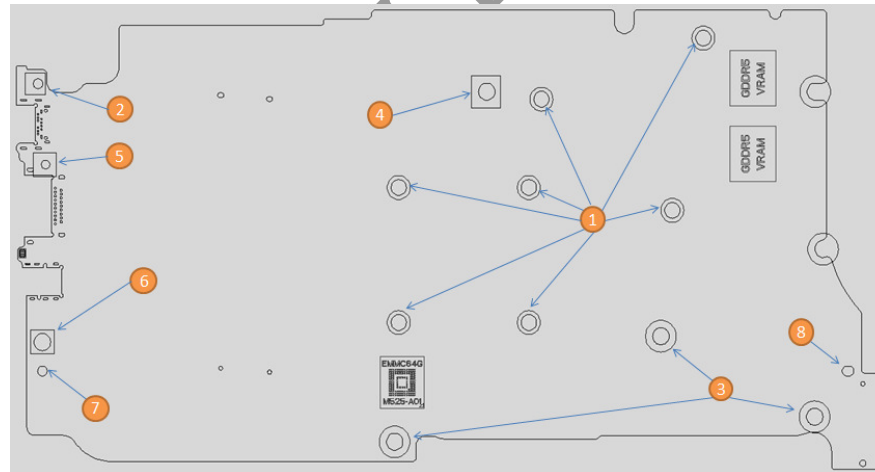
PTH Hole



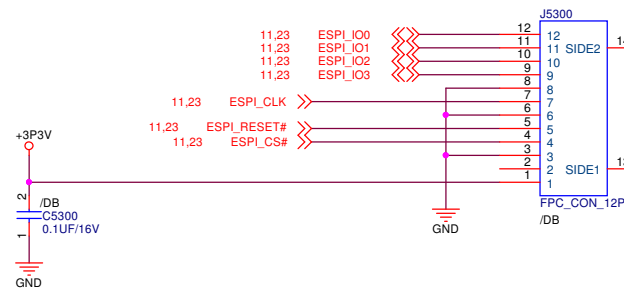
NPTH Hole



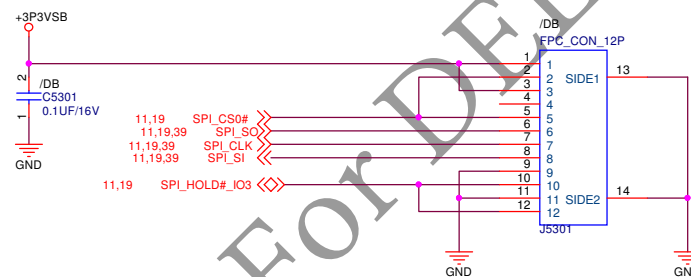
	Ø	TOP PAD	BTM PAD	PTH/NPTH	REMARK
1	Ø=4.0	Ø=6.0	Ø=4.4	PTH	THERMAL BRKT
2	Ø=2.5	L=5.3	L=5.3	PTH	SCREW HOLE
3	Ø=4.3	Ø=8.0	Ø=8.0	PTH	SCREW HOLE
4	Ø=4.3	L=7.5	Ø=8.0	PTH	SCREW HOLE
5	Ø=2.2	L=5.9	L=5.9	PTH	SCREW HOLE
6	Ø=5.2	L=6.4	Ø=8	PTH	SCREW HOLE
7	Ø=2.5	N/A	N/A	NPTH	PCB FIXTURE
8	L=3.0 X Ø=2.5	N/A	N/A	NPTH	PCB FIXTURE



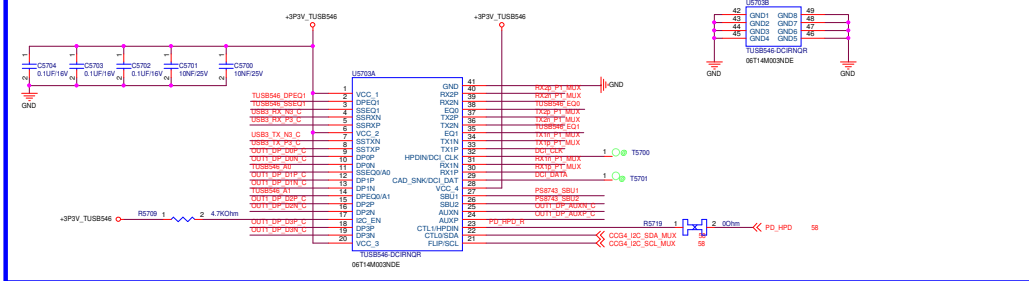
eSPI DEBUG PORT



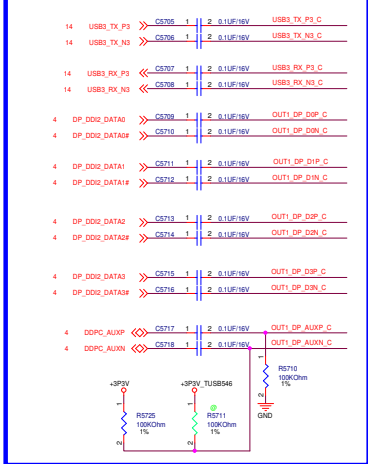
For BIOS Flash ROM



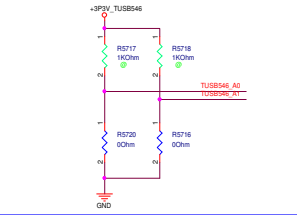
MUX



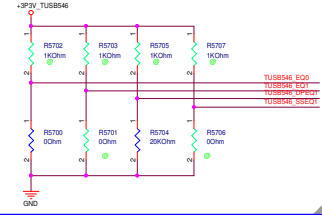
PCH Side



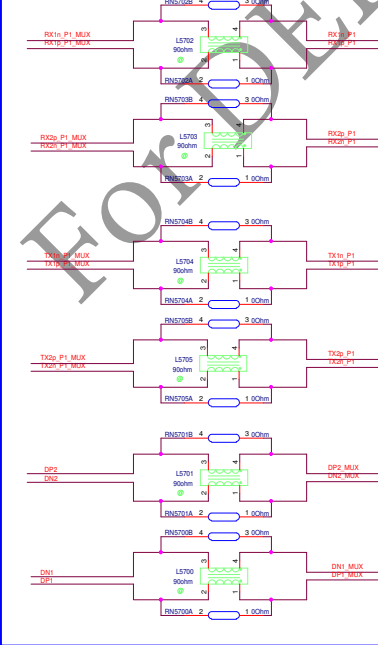
ADDRESS



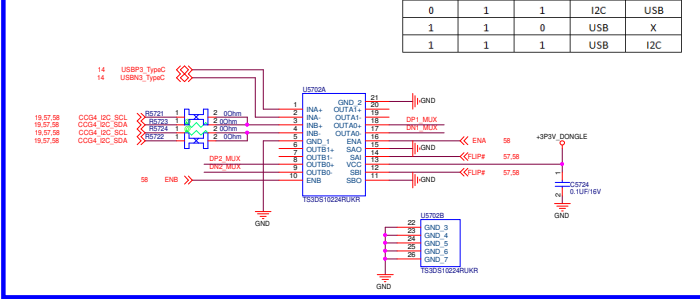
EQ STRAP



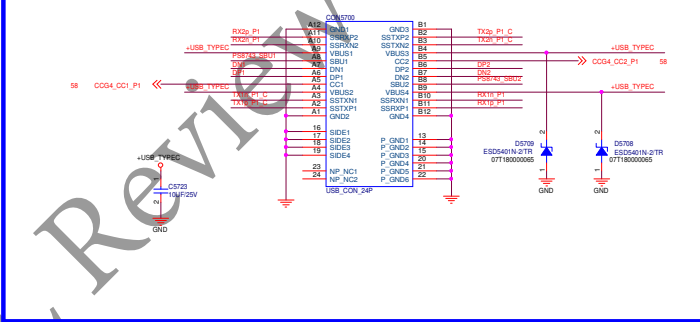
CMC



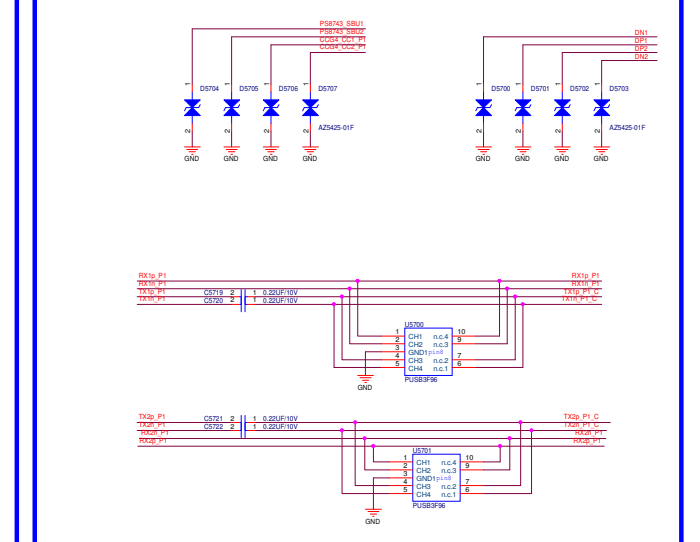
Dongle



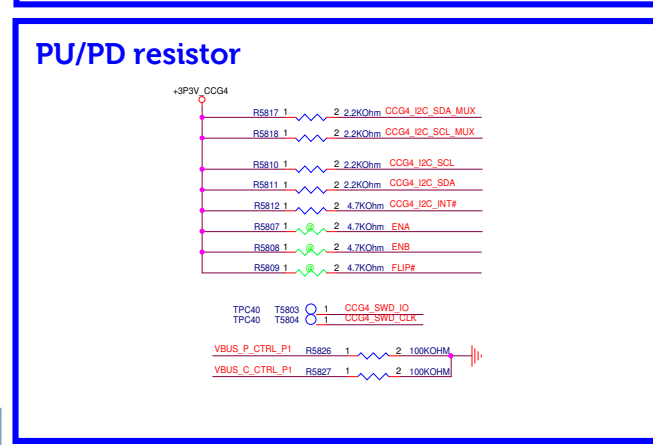
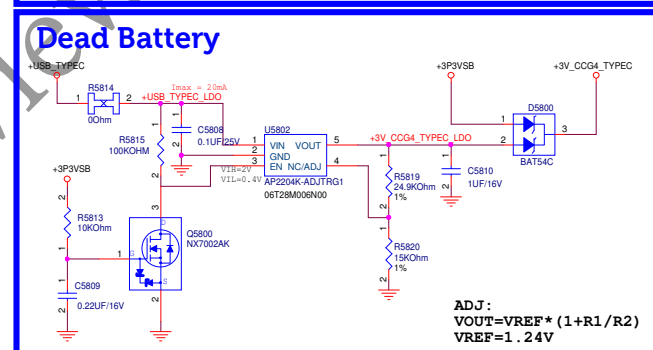
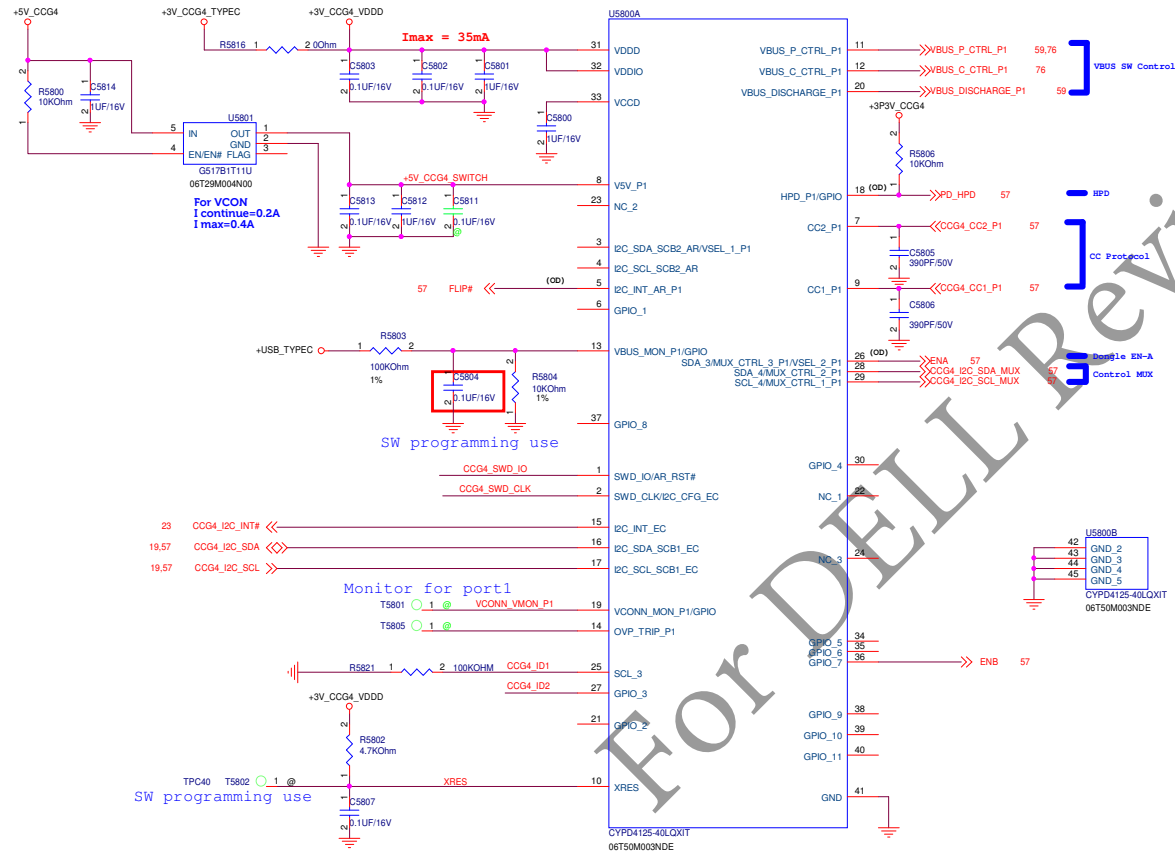
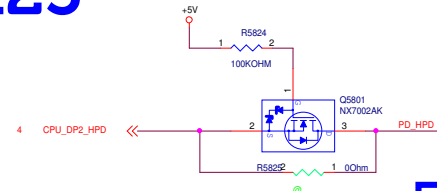
Type-C CONN



ESD

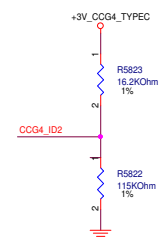


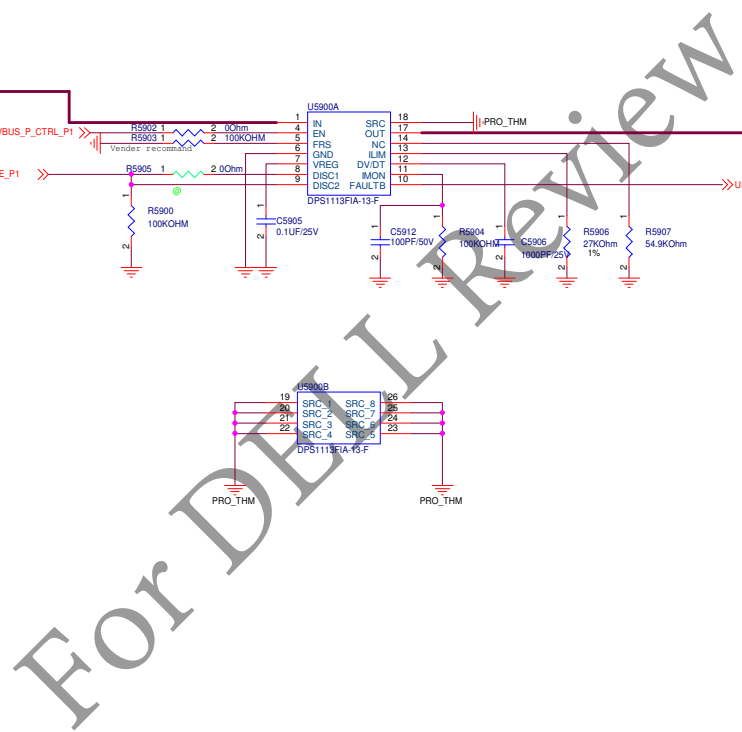
PD-CYPD4125



#	Platform	Voltage on CCG4_ID_1	Voltage on CCG4_ID_2
1	Single Port - Intel - DDM support - Armani 13" & 14"	L0	L7
2	Single Port - Intel - DDM support - Kyloren	L0	L6
3	Single Port - Intel - DDM support - Miyake	L0	L5
4	Single Port - Intel - DDM support - Loki 13"	L0	L4
5	Single Port - Intel - DDM support - Loki 15" & 17" (Motherboard is same)	L0	L3
6	Single Port - Intel - DDM support - StarLord KBL - R	L0	L2
7	Single Port - AMD - DDM not supported - Loki 15" & 17" (Motherboard is same)	L4	L0

Voltage level	Voltage value
L0	0V
L1	3.3V/8
L2	2 * 3.3V/8
L3	3 * 3.3V/8
L4	4 * 3.3V/8
L5	5 * 3.3V/8
L6	6 * 3.3V/8
L7	7 * 3.3V/8





For DELL Review

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : dGPU_IFPA/B LVDS

Pegatron Corp. Engineer: .

Size A4	Project Name Loki/Armani	Rev A00
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Date: Friday, August 25, 2017 Sheet 61 of 999

Straps Mapping

Table 3–22 Multi-level Pin Straps

MLPS Bit	Strap Name	Description	Recommended Settings
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. See Primary Memory Aperture Size (p. 26) .	Design dependent, see the description.
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	N/A	Reserved.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent, see the description.

PS_1[2]	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-/half-swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	PCI EXPRESS® transmitter, de-emphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_2[4]	N/A	Reserved.	1
PS_2[5]	N/A	Reserved.	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID	Design dependent, see the description.
PS_3[4]	N/A	Reserved.	1
PS_3[5]	N/A	Reserved.	1

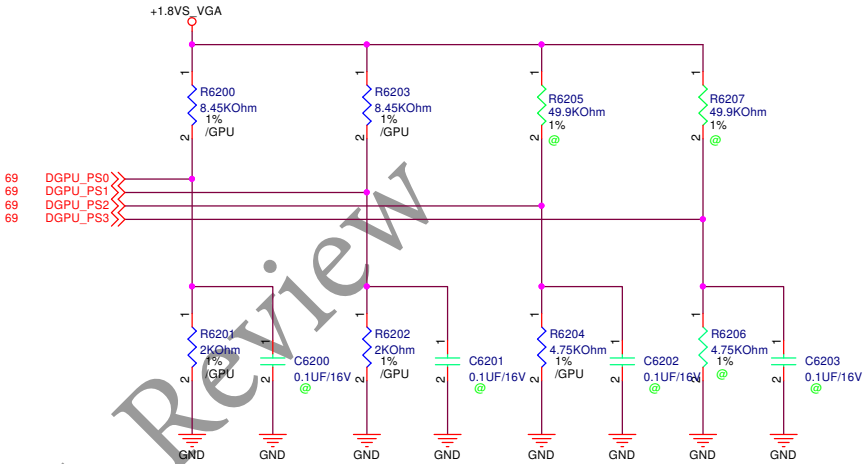


Table 3–23 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

Table 3–21 Resistor Divider Lookup Table for Bits [3:1]

R _{pu} (Ω)	R _{pd} (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Table 3–20 Capacitor Lookup Table for Bits [5:4]

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

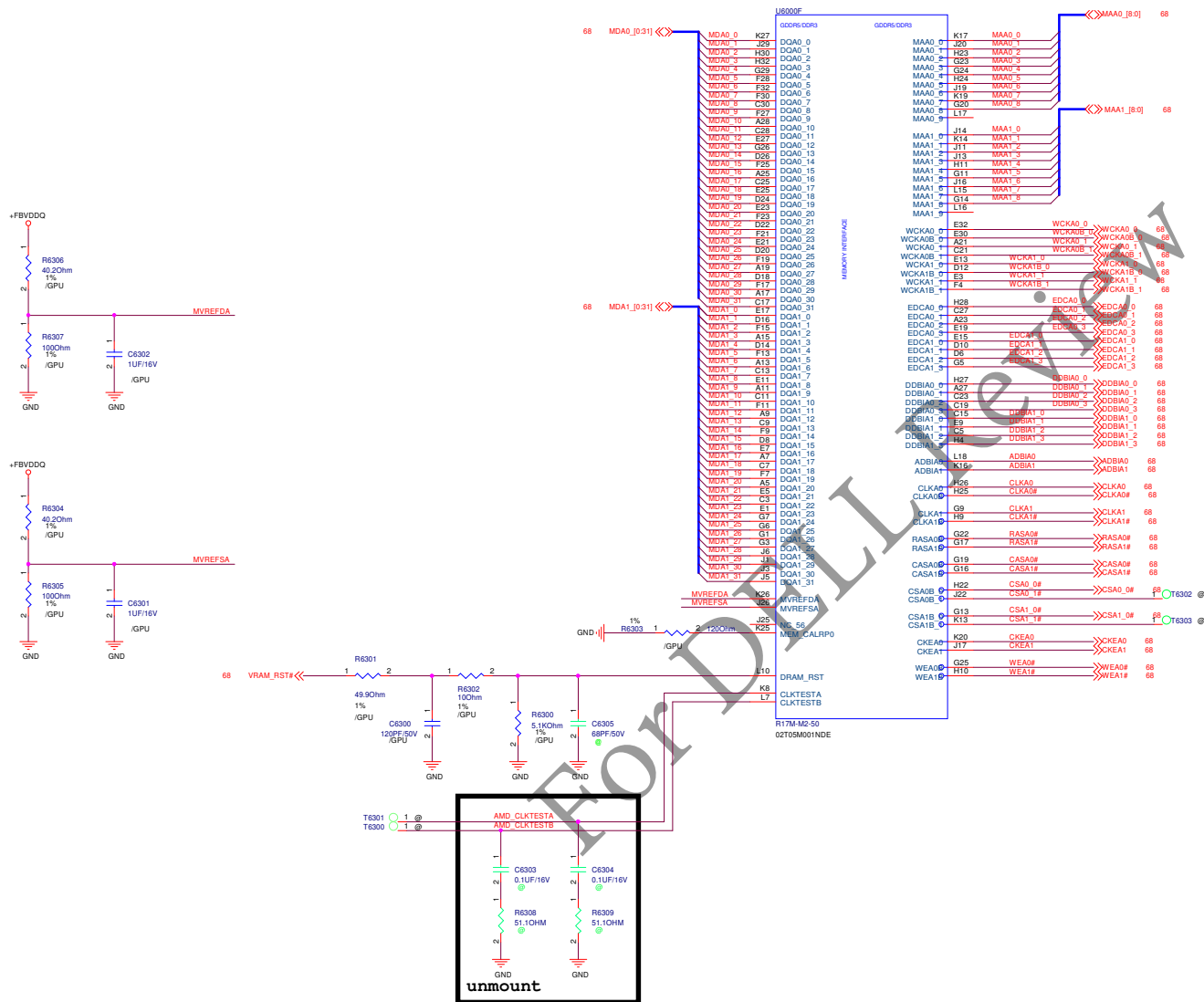
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **dGPU STRAPS**

Pegatron Corp. Engineer: .

Size A3 Project Name **Loki/Armani** Rev A00

Date: Friday, August 25, 2017 Sheet 62 of 999



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : dGPU FBA

Pegatron Corp.		Engineer: .	
Size	Project Name	Rev	
A2	Loki/Armani	A00	
Date: Friday, August 25, 2017		Sheet	63 of 99

For DELL Review

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PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : dGPU_FBVDDQ

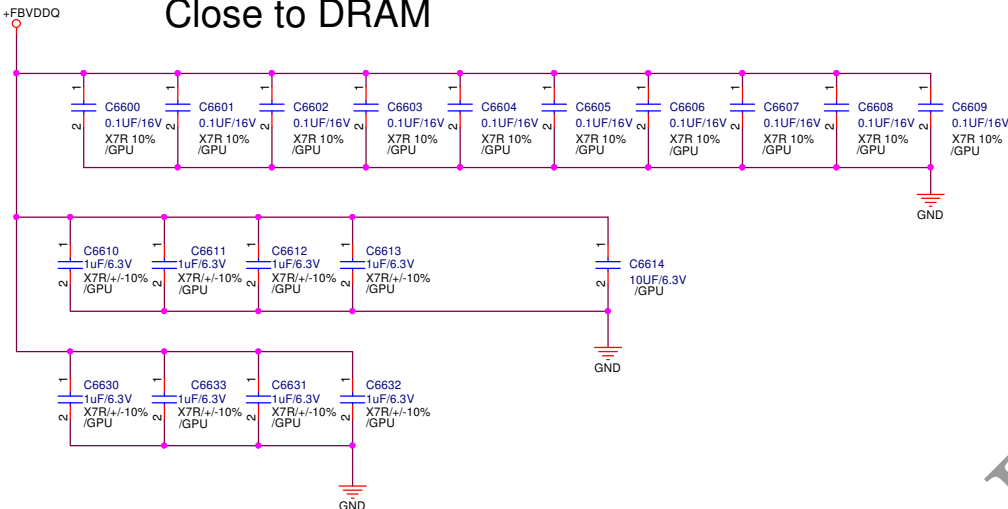
Pegatron Corp. Engineer: .

Size A3	Project Name Loki/Armani	Rev A00
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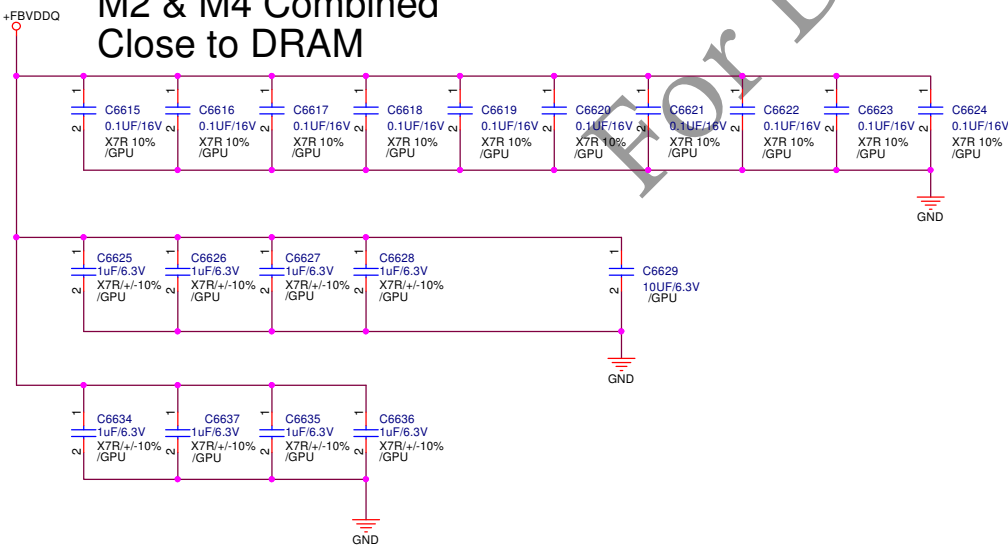
Memory FBVDD/Q Decoupling

M1 & M3 Combined Close to DRAM



Capacitor Type		Footprint		Population ¹		Location ²
				FBVDDQ	FBVDD	
FBVDD/Q Combined						
0.1 μF	X7R	0402	10	10		Under DRAM
1.0 μF	X7R	0603	4	4		Under DRAM
10 μF	X5R	0805	2	2		Close to DRAM
FBVDD/Q Separate						
0.1 μF	X7R	0402	6	6	0	Under DRAM
1.0 μF	X7R	0603	8	4	4	Under DRAM
10 μF	X5R	0805	2	1	1	Close to DRAM
Note:						
1. Per sub-partition, for example, per two pieces of ×16 DRAM or one piece of ×32 DRAM.						
2. Location is close to DRAM for all decoupling with ×16 DRAM.						

M2 & M4 Combined Close to DRAM



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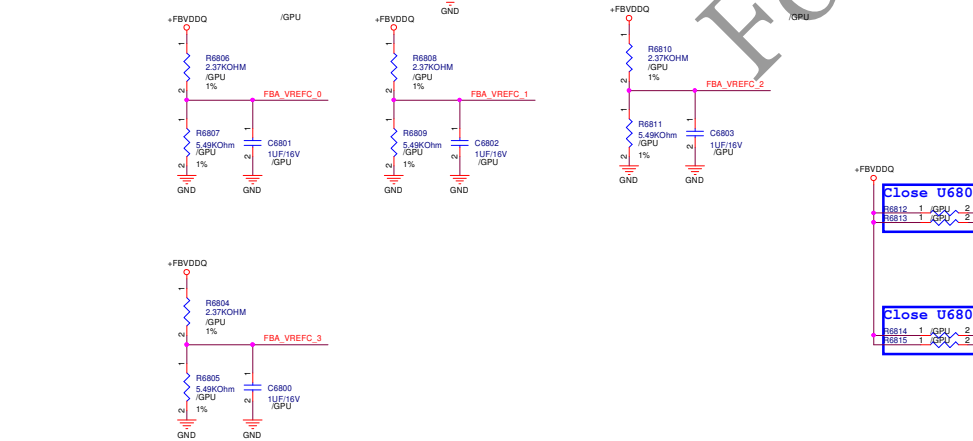
PEGATRON Title : dGPU MEMORY DECOU

Pegatron Corp. Engineer: .

Size A3 Project Name Loki/Armani Rev A00

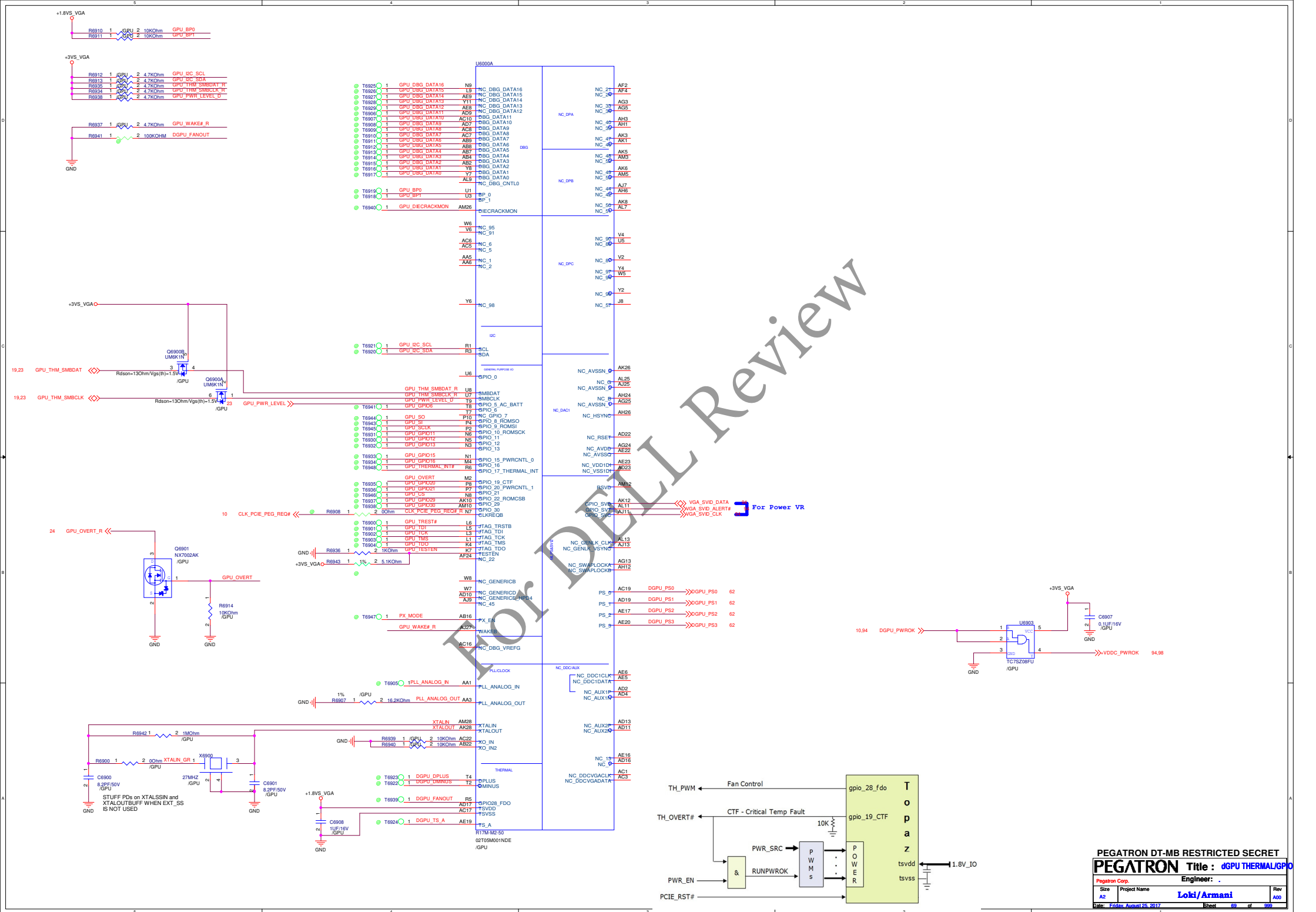
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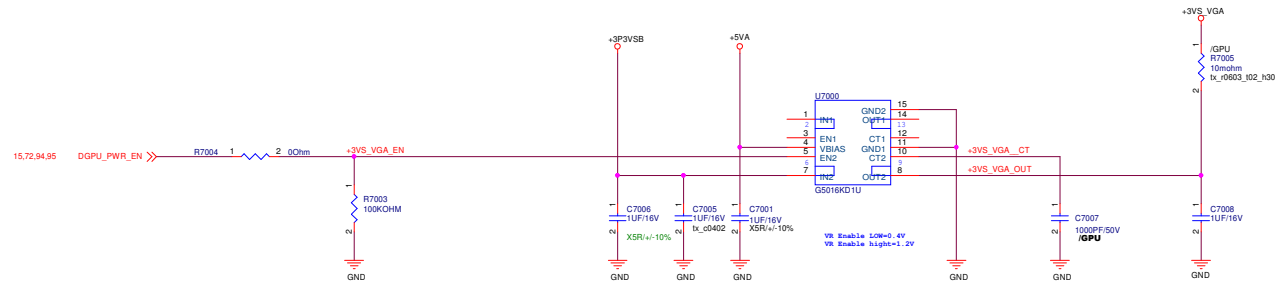
BYTE 1



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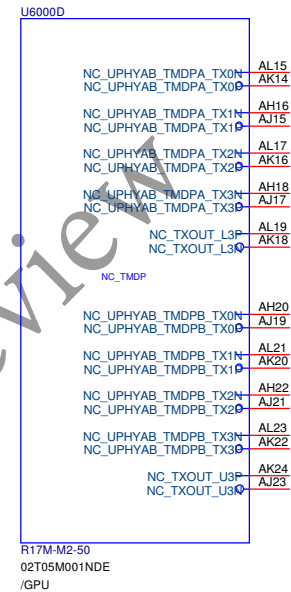
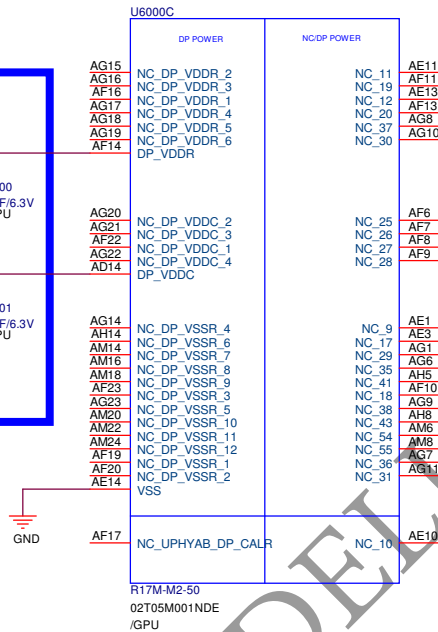
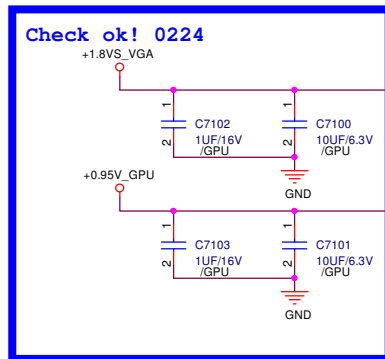
PEGATRON Title : 70.VRAM_SELF_REFRESH

Pegatron Corp. Engineer: .

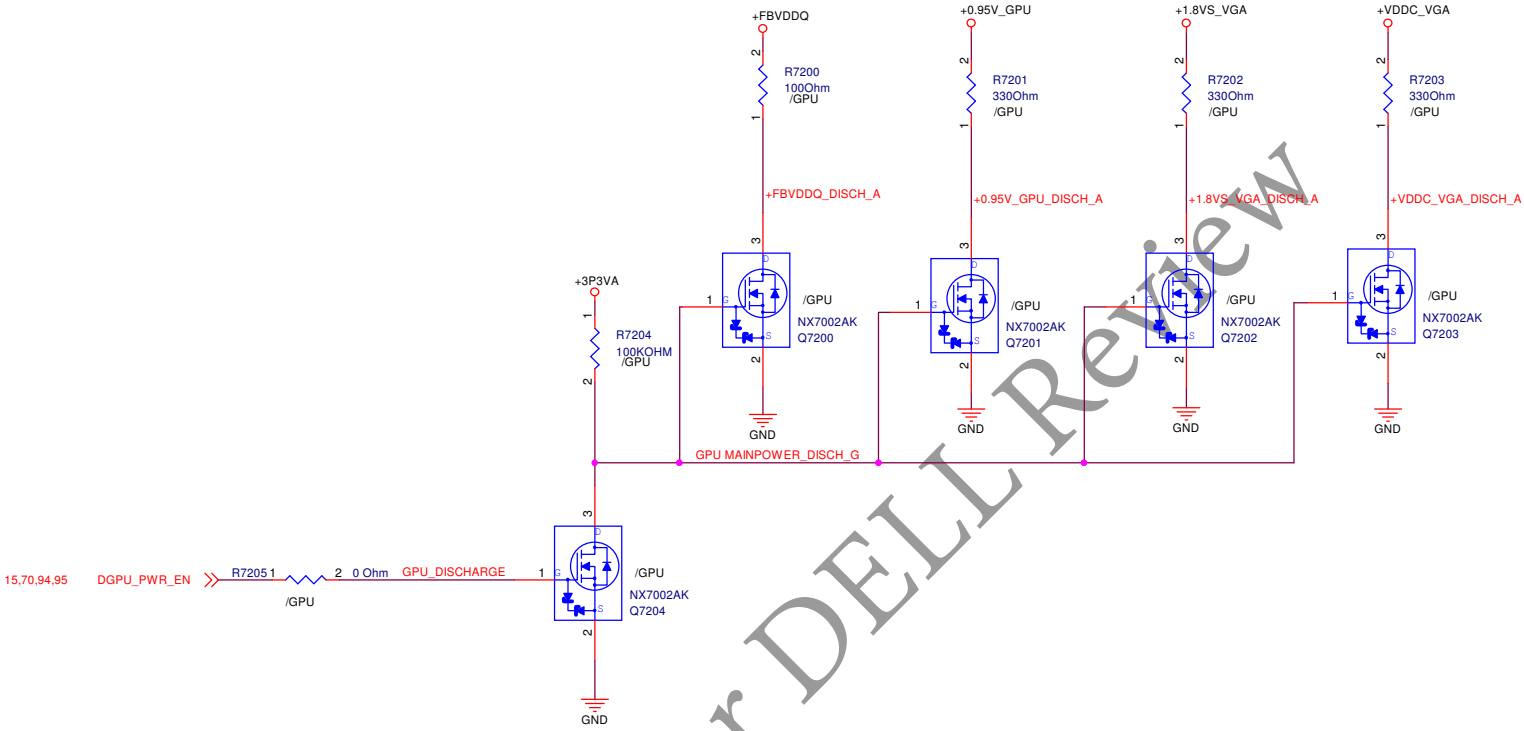
Size Project Name

A2 Loki/Armani Rev

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GPU POWER DISCHARGE



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : GPU POWER DISCHARGE

Pegatron Corp. Engineer: .

Size A3	Project Name Loki/Armani	Rev A00
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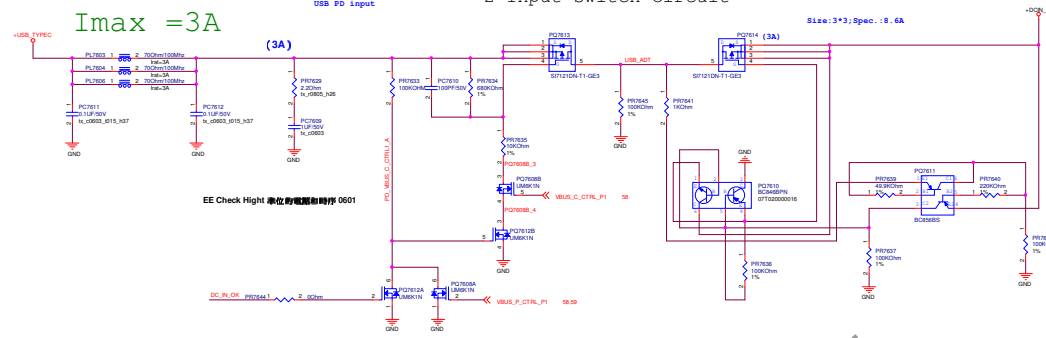
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VBUS Consumer

$I_{max} = 3A$

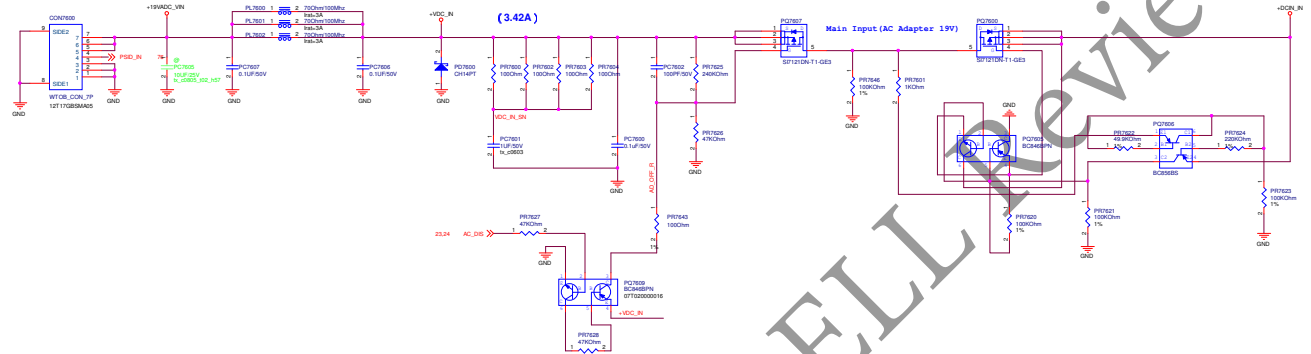
2nd Input (USB PD 50V)
USB PD Input

2 Input switch Circuit

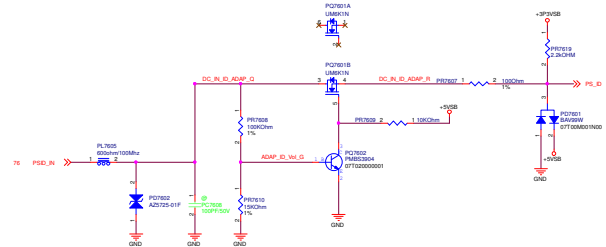


DC-IN connector

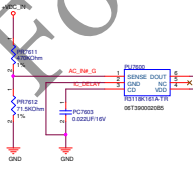
$I_{max} = 3.42A$



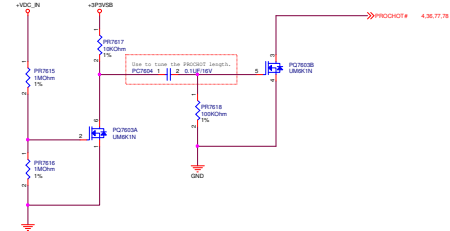
PSID Circuit



HW_ACAVIN_NB Circuit

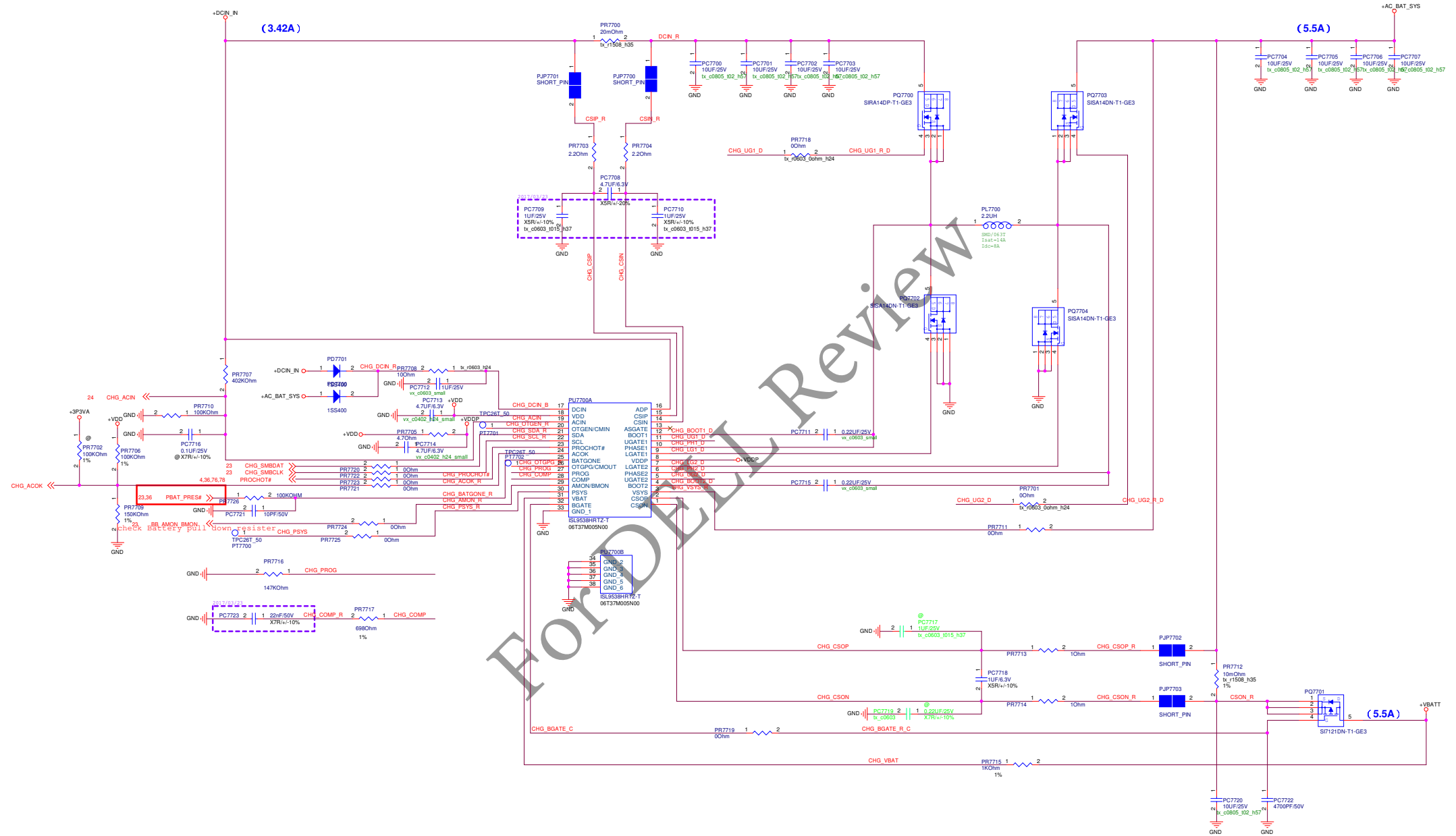


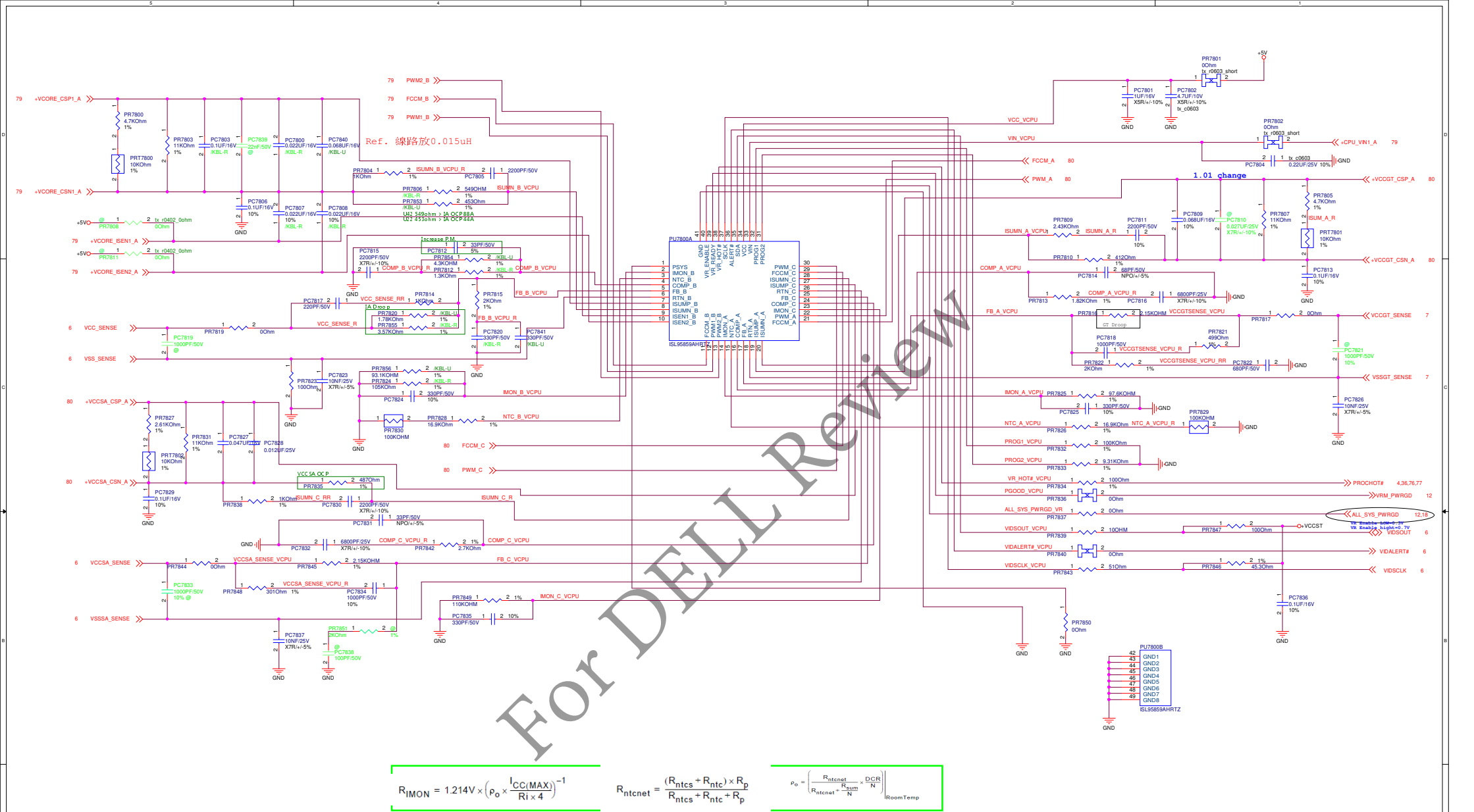
Battery Protect Circuit



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : DC-IN
Project Name	Engineer : -	
Drawn	Loki/Armani	Rev
Check	Armani	App





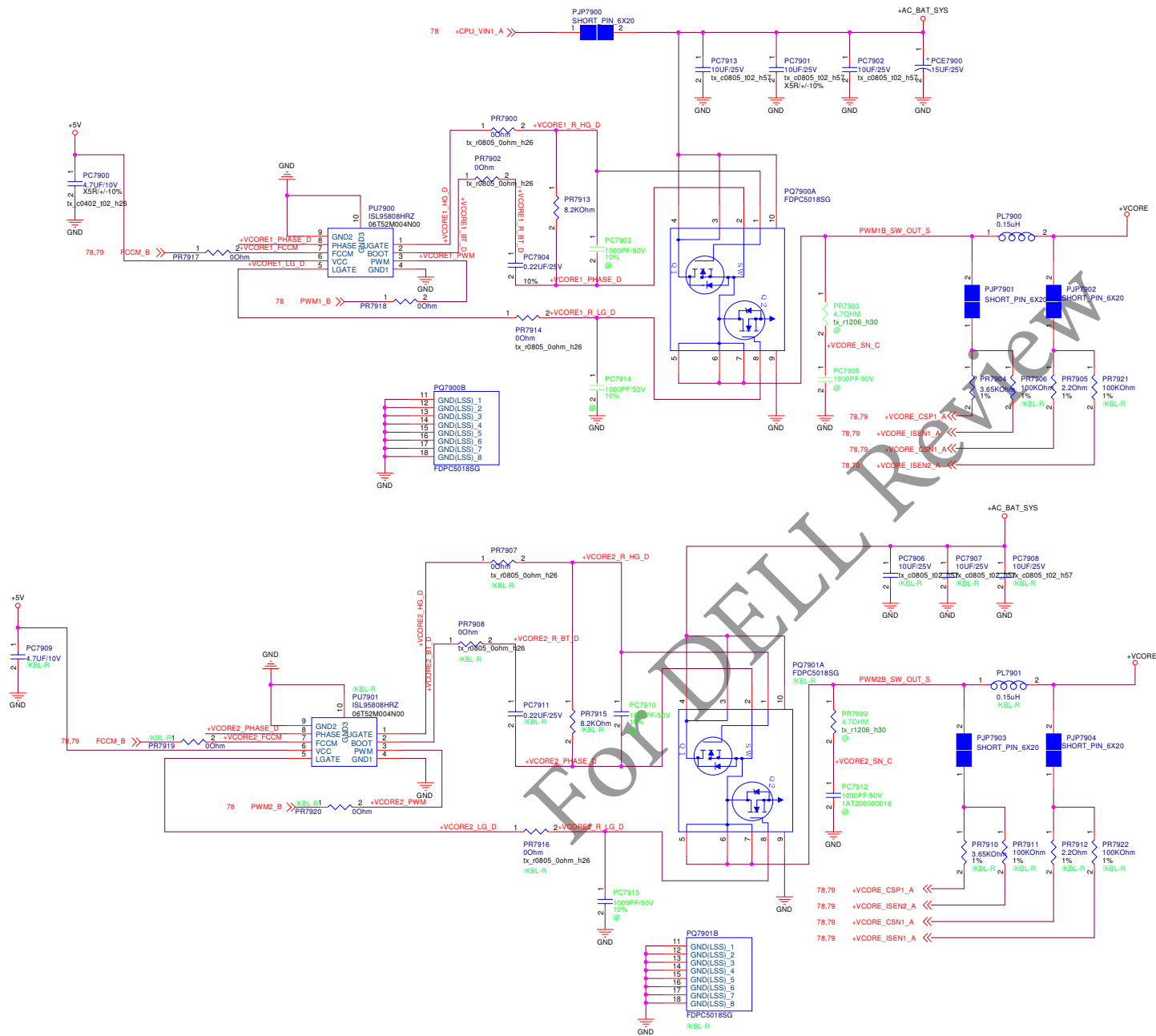
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU CONTROLLER

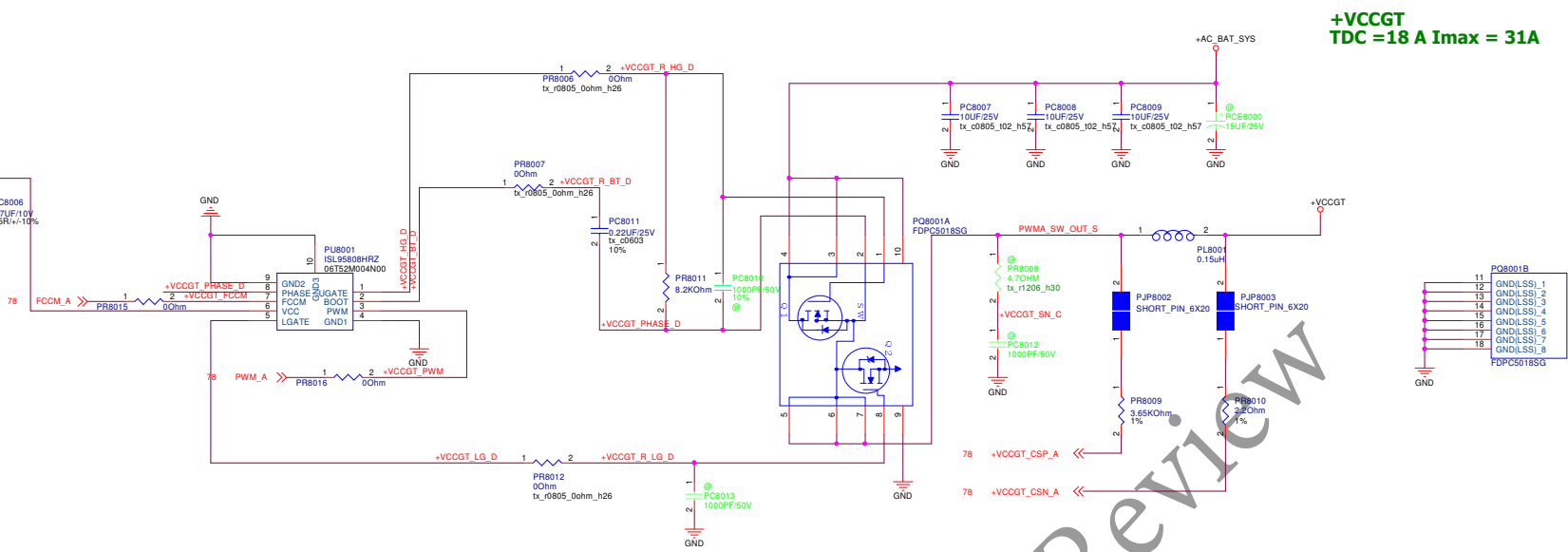
Pegatron Corp. Engineer : .

Size	Project Name	Rev
A2	Loki/Armani	A00

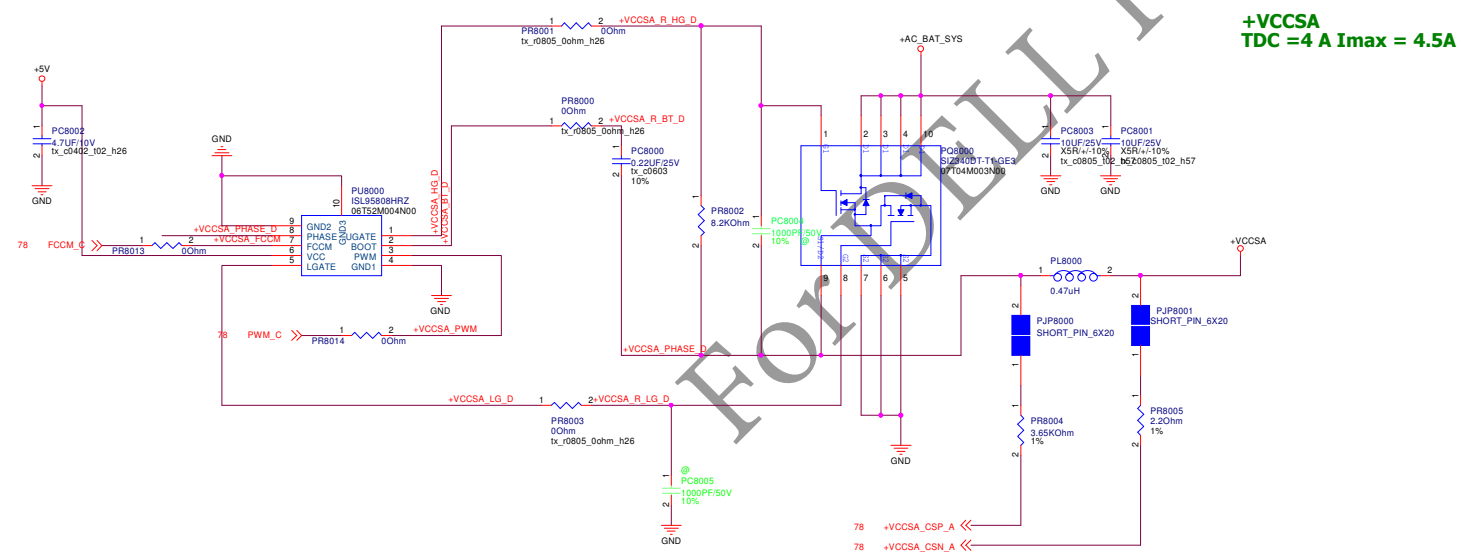
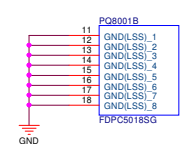
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+Vcore
TDC = 42A Imax = 64A

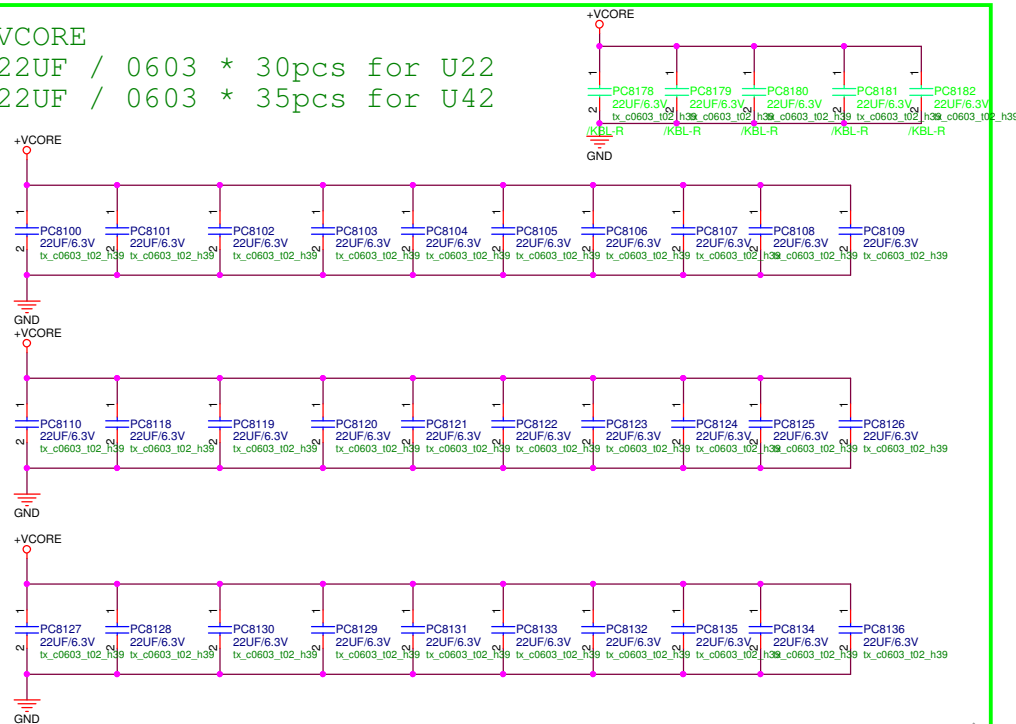


+VCCGT
TDC = 18 A Imax = 31A

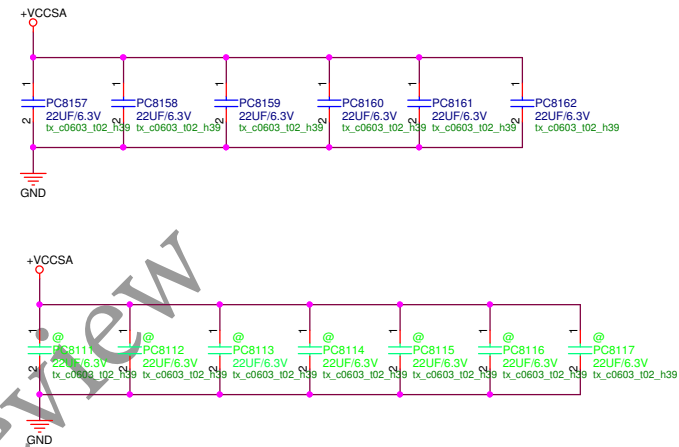


+VCCSA
TDC = 4 A Imax = 4.5A

VCORE
22UF / 0603 * 30pcs for U22
22UF / 0603 * 35pcs for U42



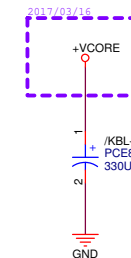
VCCSA
22UF / 0603 * 6pcs



VCCGT
22UF / 0603 * 40pcs



VCORE for KBL-R
330UF / 2V / 9m ohm * 1



PEGATRON DT-MB RESTRICTED SECRET

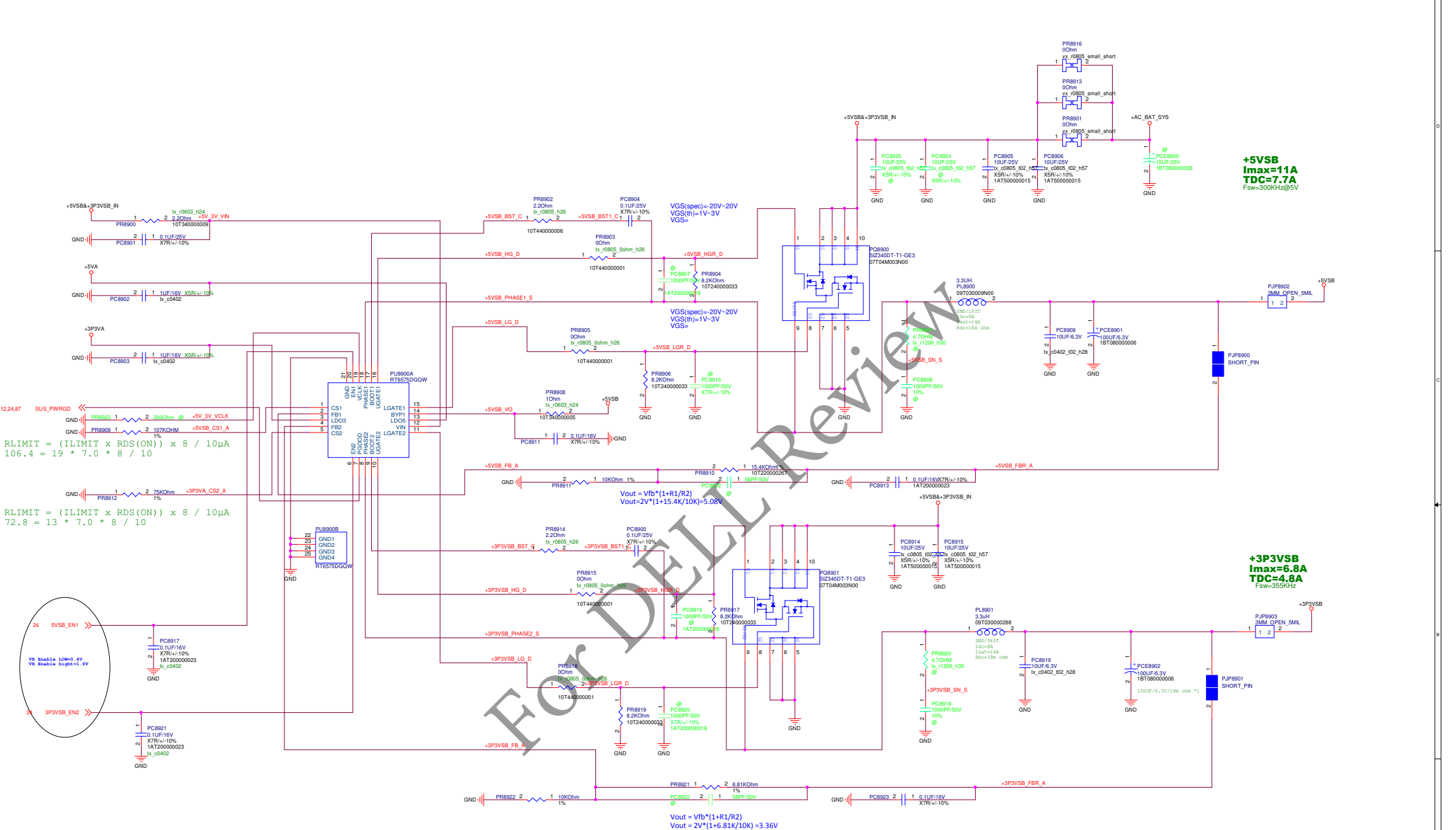
For DELL Review

For DELL Review

For DELL Review

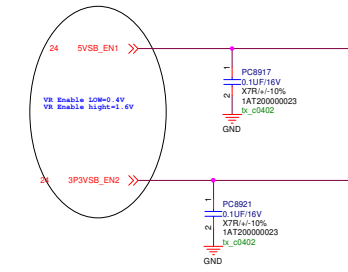
For DELL Review

PEGATRON DT-MB RESTRICTED SECRET			
PEGATRON		Title : +VCCEPIO	
Pegatron Corp.		Engineer: .	
Size	Project Name		Rev
A2	Loki/Armani		A00
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12,24,87 SUS_PWRGD <<
RLIMIT = (ILIMIT x RDS(ON)) x 8 / 10µA
106.4 = 19 * 7.0 * 8 / 10

RLIMIT = (ILIMIT x RDS(ON)) x 8 / 10µA
72.8 = 13 * 7.0 * 8 / 10



+5VSB
Imax=11A
TDC=7.7A
Fsw=300kHz@5V

+3P3VSB
Imax=6.8A
TDC=4.6A
Fsw=355kHz

$$V_{out} = V_{fb} * (1 + R1/R2)$$
$$V_{out} = 2V * (1 + 15.4K/10K) = 5.08V$$

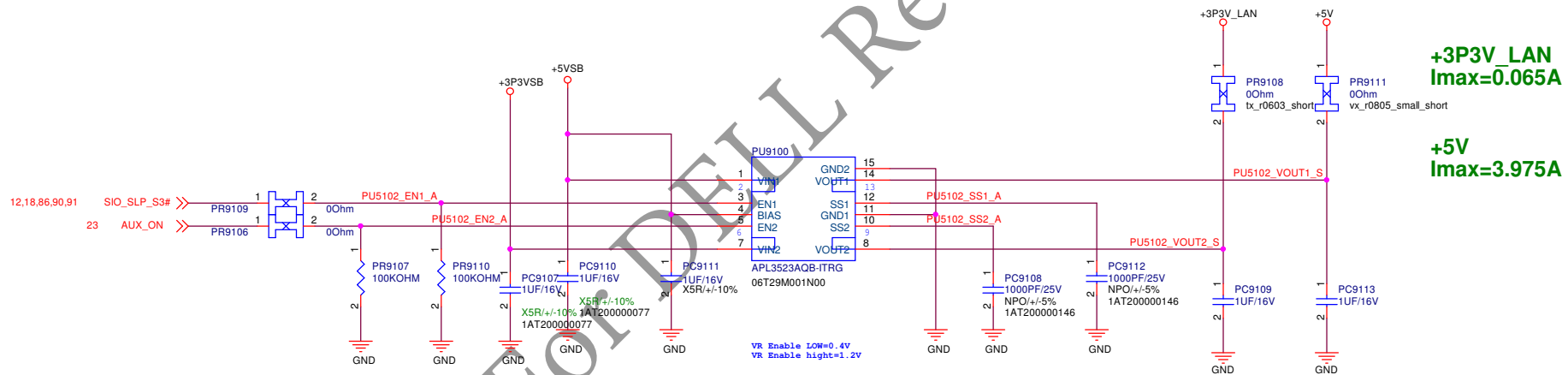
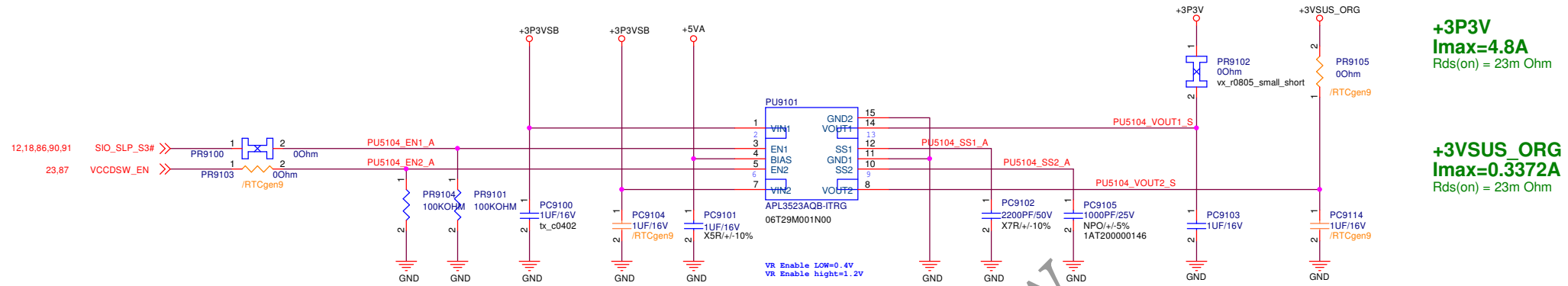
$$V_{out} = V_{fb} * (1 + R1/R2)$$
$$V_{out} = 2V * (1 + 6.81K/10K) = 3.36V$$

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **+3VA/+5VSB**

Pegatron Corp. Engineer: .
Size A2 Project Name **Loki/Armani** Rev A00

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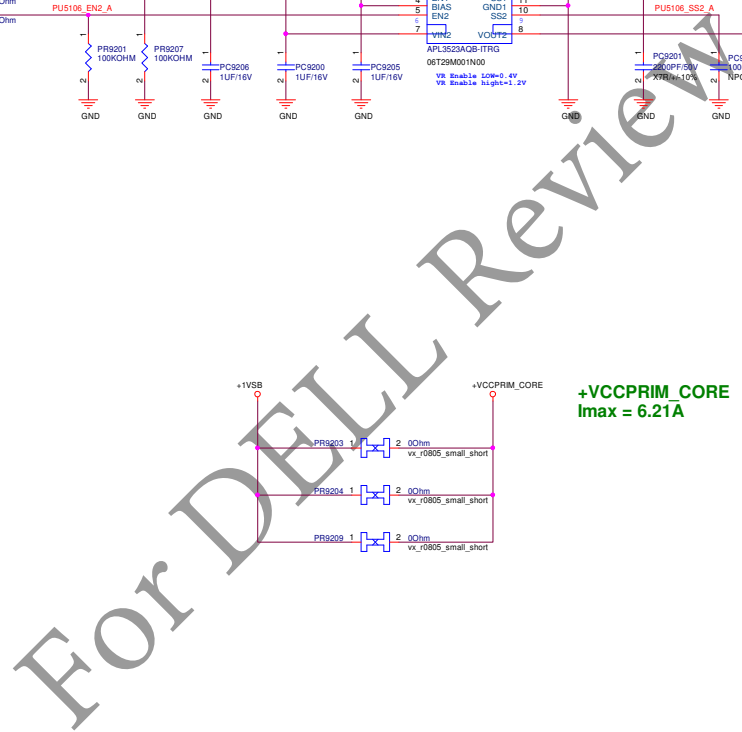
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : Load Switch 2

Pegatron Corp. Engineer: .

Size A3	Project Name Loki/Armani	Rev A00
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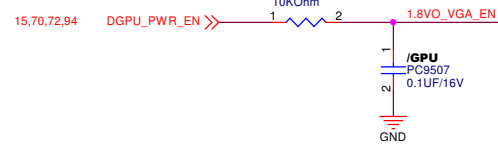
+VCCPRIM_CORE
I_{max} = 6.21A

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PEGATRON DT-MB RESTRICTED SECRET

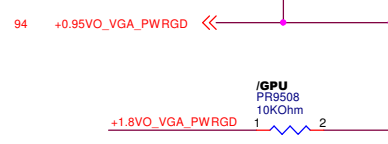
PEGATRON		Title : LD01	
Pegatron Corp.		Engineer: .	
Size A3	Project Name Loki/Armani		Rev A00
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(0.65A)



Vout=FB * (1+ (R9504 / R9508))
VFB=0.6V;T=2%

(0.65A)



$$V_{out} = V_{FB} * (1 + (R_{509} / R_{507}))$$

PEGATRON Title : +NVDD PHASE

Registration Title:

Size	Project Name	Rev
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A3	Loki/Armani	A00
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For DELL Review

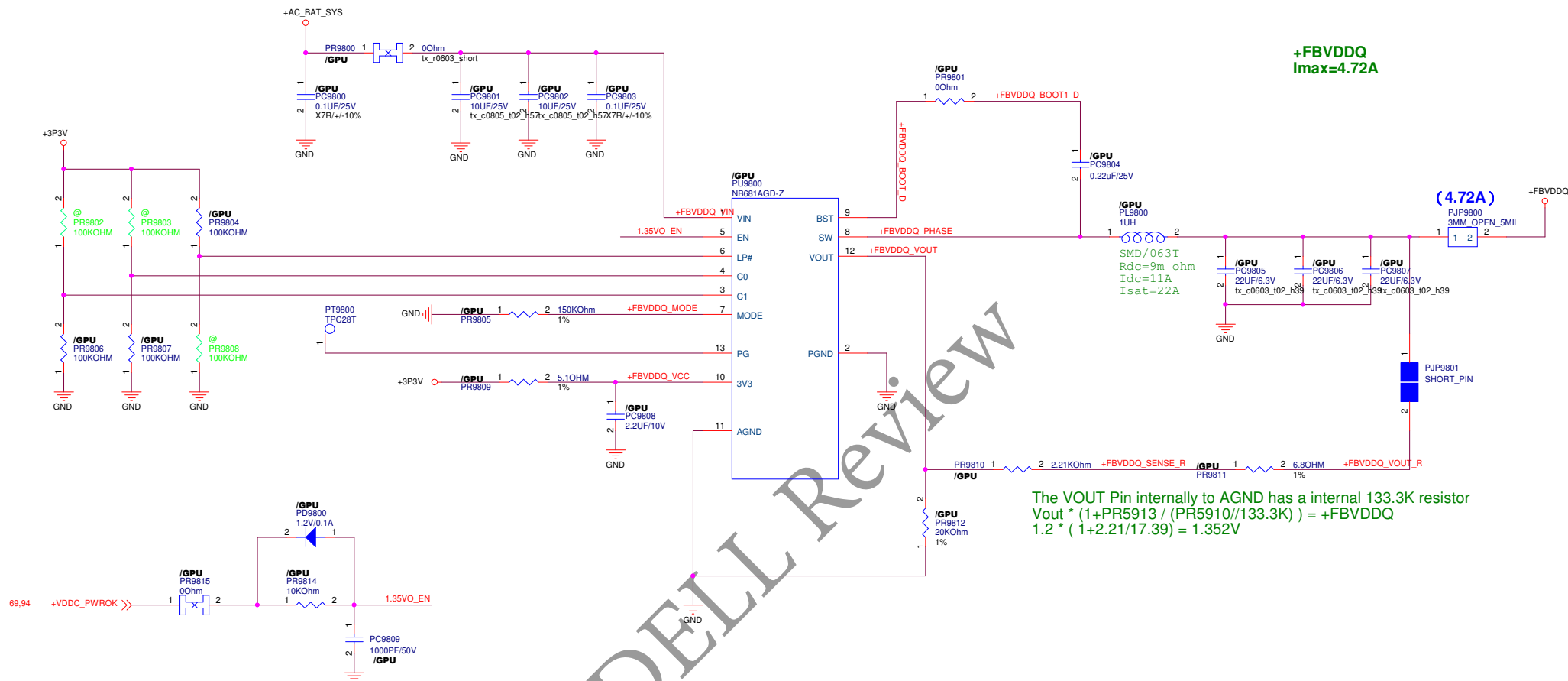
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **+1P05VSB**

Pegatron Corp. Engineer: .

Size	Project Name	Rev
A3	Loki/Armani	A00

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	LP#	C1	C0	VOUT(V)
Others (Fixed design only, not allowed for changing on-the-fly)	0	0	0	1.59
	0	0	1	1.99
	0	1	0	2.38
	0	1	1	3.3
	1	0	0	1.2
	1	0	1	1.5
	1	1	0	1.8
	1	1	1	2.5

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON			Title :	FBVDDQ
Pegatron Corp.			Engineer:	.
Size	Project Name			Rev
Custom	Loki/Armani			A00
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